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S1D13700F01
Embedded Memory Graphics LCD Controller

Hardware Functional Specification

Document Number: X42A-A-002-04

Status: Revision 4.03

Issue Date: 2005/06/01

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1 Introduction

1.1 Scope

This is the Hardware Functional Specification for the S1D13700F01. Included in this document are timing diagrams, AC and DC characteristics, register descriptions, and power management descriptions. This document is intended for two audiences: Video Subsystem Designers and Software Developers.

This document is updated as appropriate. Please check the Epson Research and Development Website at **www.erd.epson.com** for the latest revision of this document before beginning any development.

We appreciate your comments on our documentation. Please contact us via email at documentation@erd.epson.com.

1.2 Overview Description

The S1D13700F01 can display both text and graphics on an LCD panel. The S1D13700F01 allows layered text and graphics, scrolling of the display in any direction, and partitioning of the display into multiple screens. It includes 32K bytes of embedded SRAM display memory which is used to store text, character codes, and bit-mapped graphics. The S1D13700F01 handles display controller functions including: transferring data from the controlling microprocessor to the buffer memory, reading memory data, converting data to display pixels, and generating timing signals for the LCD panel.

The S1D13700F01 is designed with an internal character generator which supports 160, 5x7 pixel characters in internal mask ROM (CGROM) and 64, 8x8 pixel characters in character generator RAM (CGRAM). When the CGROM is not used, up to 256, 8x16 pixel characters are supported in CGRAM.

2 Features

2.1 Internal Memory

- Embedded 32K bytes of SRAM display memory

2.2 Host CPU Interface

- Direct Address Bus support for:
  - Generic Bus (Z80 family) microprocessor interface
  - MC68K family microprocessor interface
- Indirect Address Bus support for:
  - Generic Bus (Z80 family) microprocessor interface
  - MC68K family microprocessor interface
  - M6800 family microprocessor interface
- 8-bit CPU data bus interface

2.3 Display Support

- 4-bit monochrome LCD interface
- Maximum resolutions supported:
  640x240 at 1 bpp
  320x240 at 2 bpp
  240x160 at 4 bpp
- 1/2-duty to 1/256-duty LCD drive

2.4 Display Modes

- 1/2/4 bit-per-pixel color depth support
- Text, graphics and combined text/graphics display modes
- Three overlapping screens in graphics mode
- Programmable cursor control
- Smooth horizontal scrolling of all or part of the display in monochrome mode
- Smooth vertical scrolling of all or part of the display in all modes

2.5 Character Generation

- 160, 5x7 pixel characters in embedded mask-programmed character generator ROM (CGROM)
- Up to 64, 8x8 pixel characters in character generator RAM (CGRAM)
- Up to 256, 8x16 pixel characters in embedded character generator RAM (when CGROM is not used)

2.6 Power

- Software initiated power save mode
- Low power consumption
- CORE V_{DD} 3.0 to 3.6 volts
- IO V_{DD} 3.0 to 5.5 volts

2.7 Clock Source

- Two terminal crystal or Single Oscillator input
  Input Clock (maximum 60 MHz)
  FPSHIFT Clock (maximum 15 MHz)

2.8 Package

- TQFP13 - 64-pin Pb-free package (lead free)

3 System Diagrams

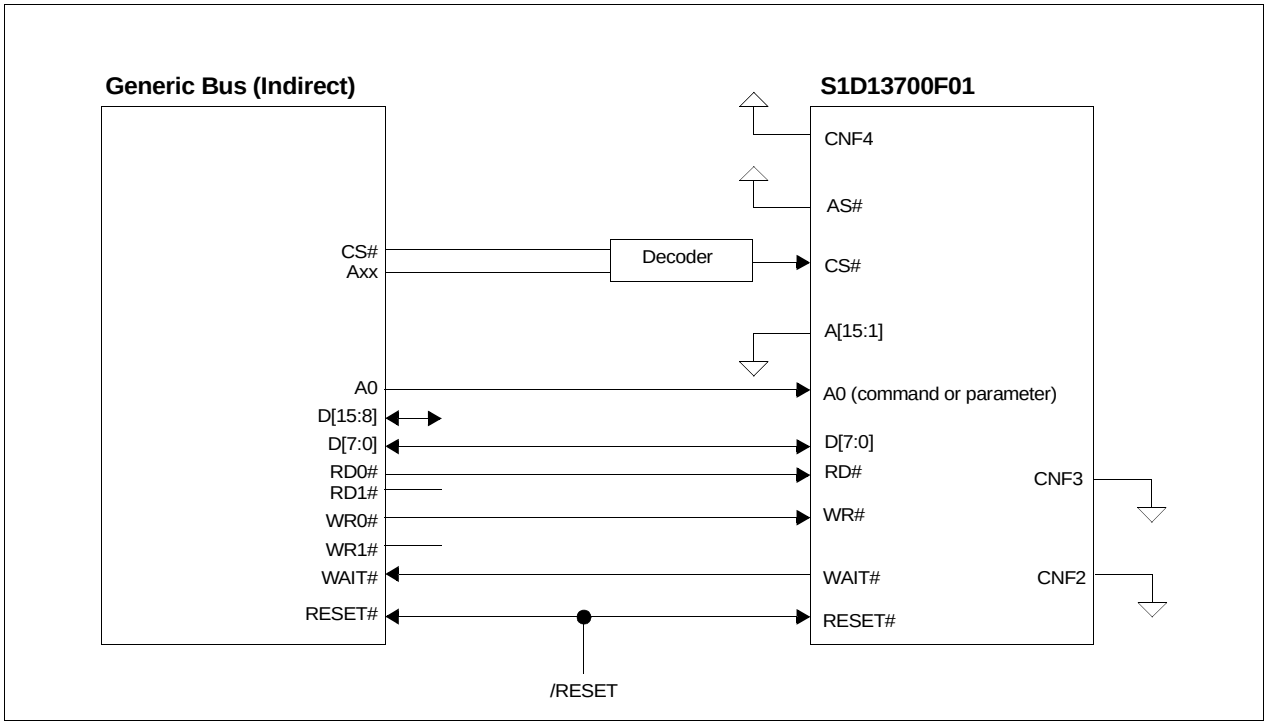


Figure 3-1 Indirect Generic to S1D13700F01 Interface Example

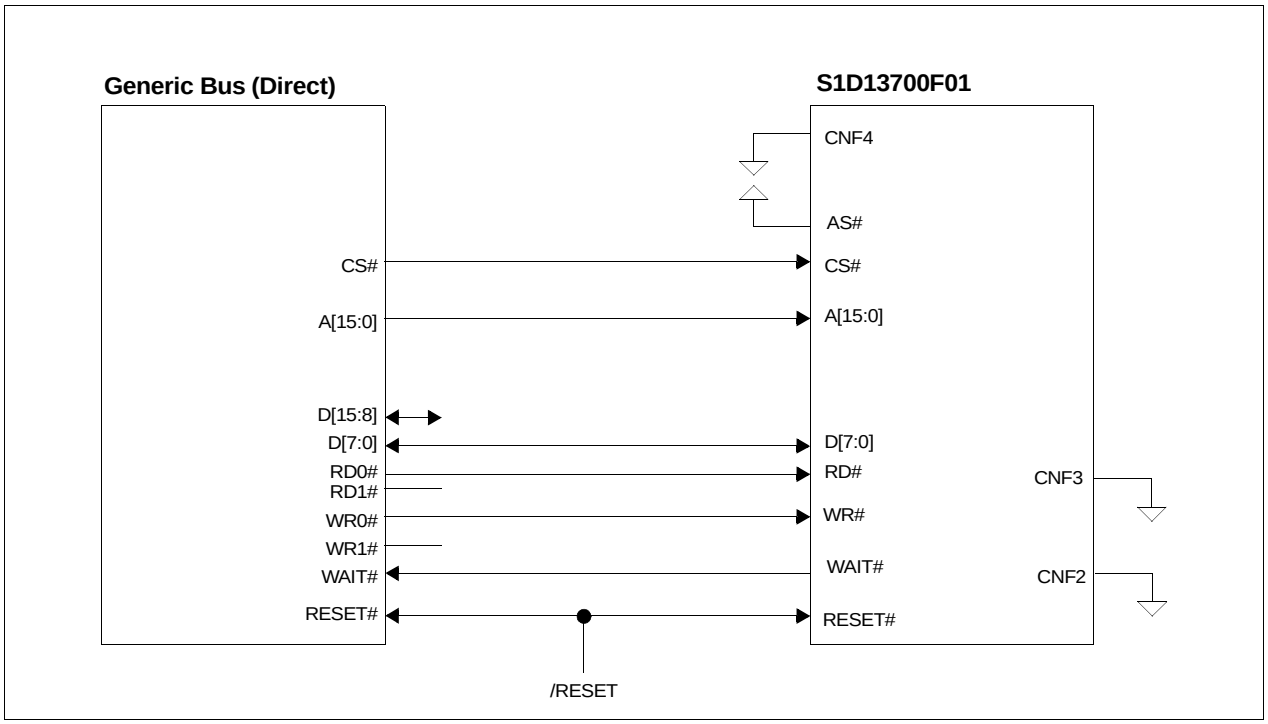


Figure 3-2 Direct Generic to S1D13700F01 Interface Example

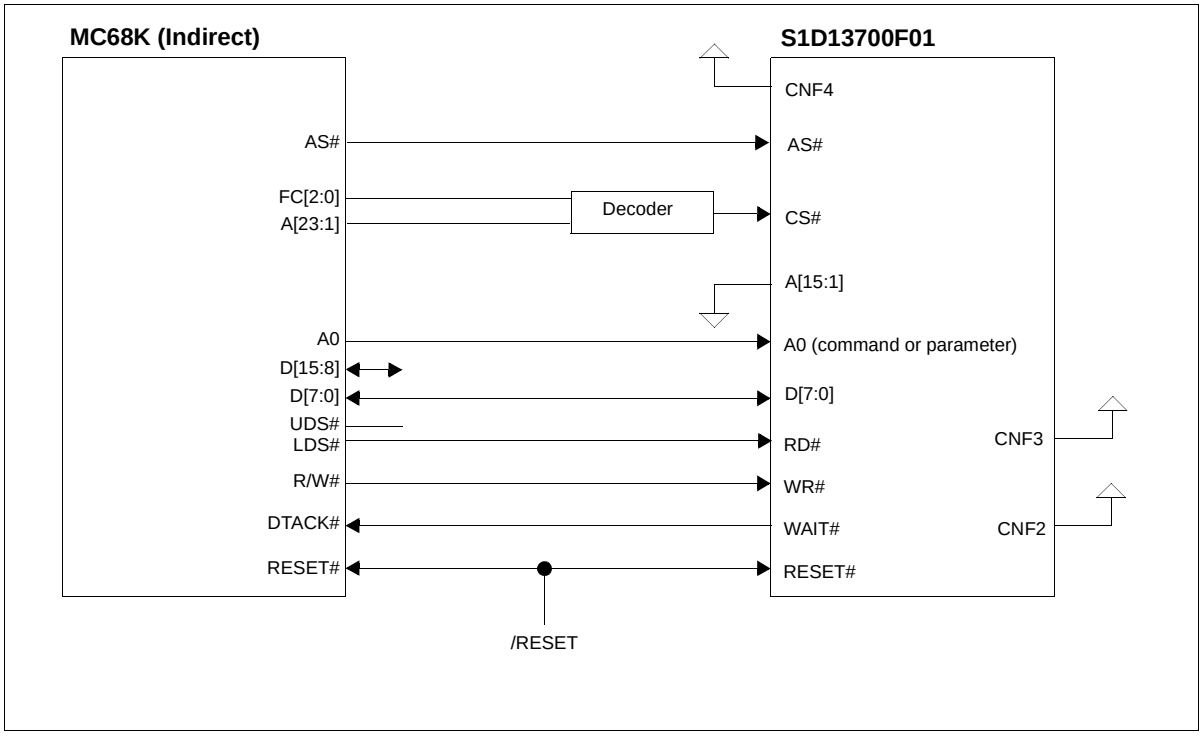


Figure 3-3 Indirect MC68K to S1D13700F01 Interface Example

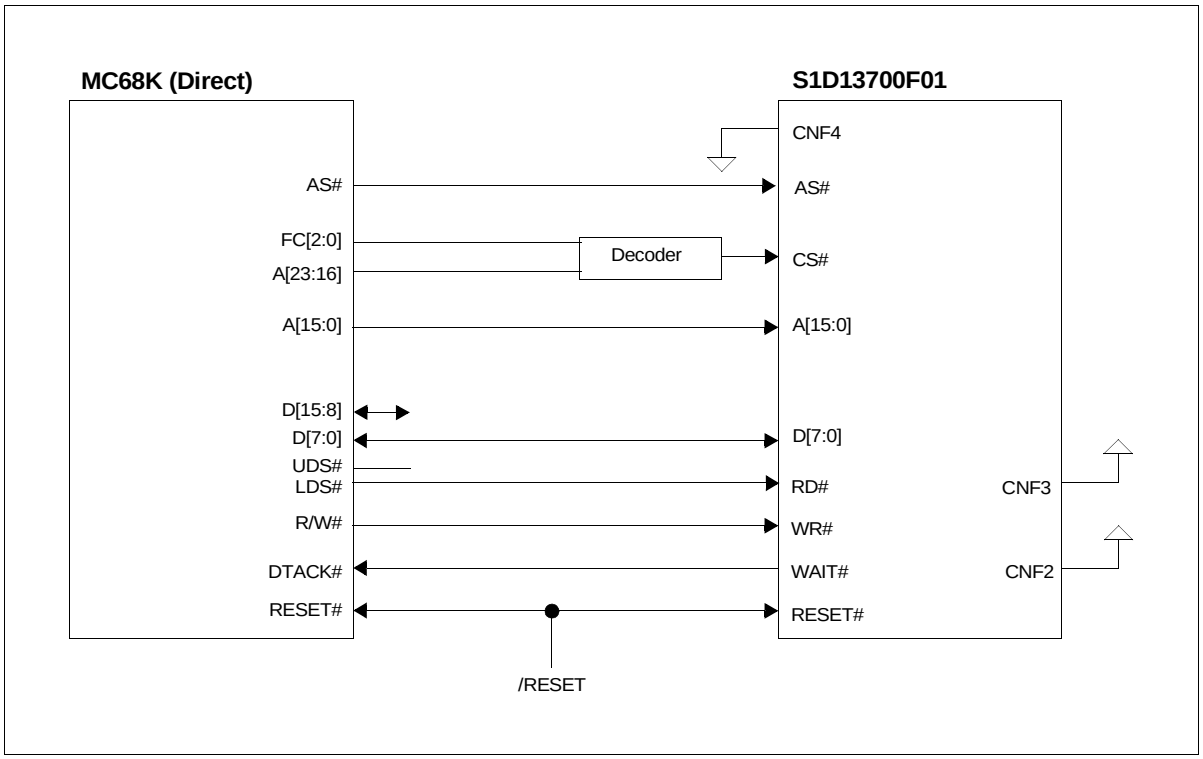


Figure 3-4 Direct MC68K to S1D13700F01 Interface Example

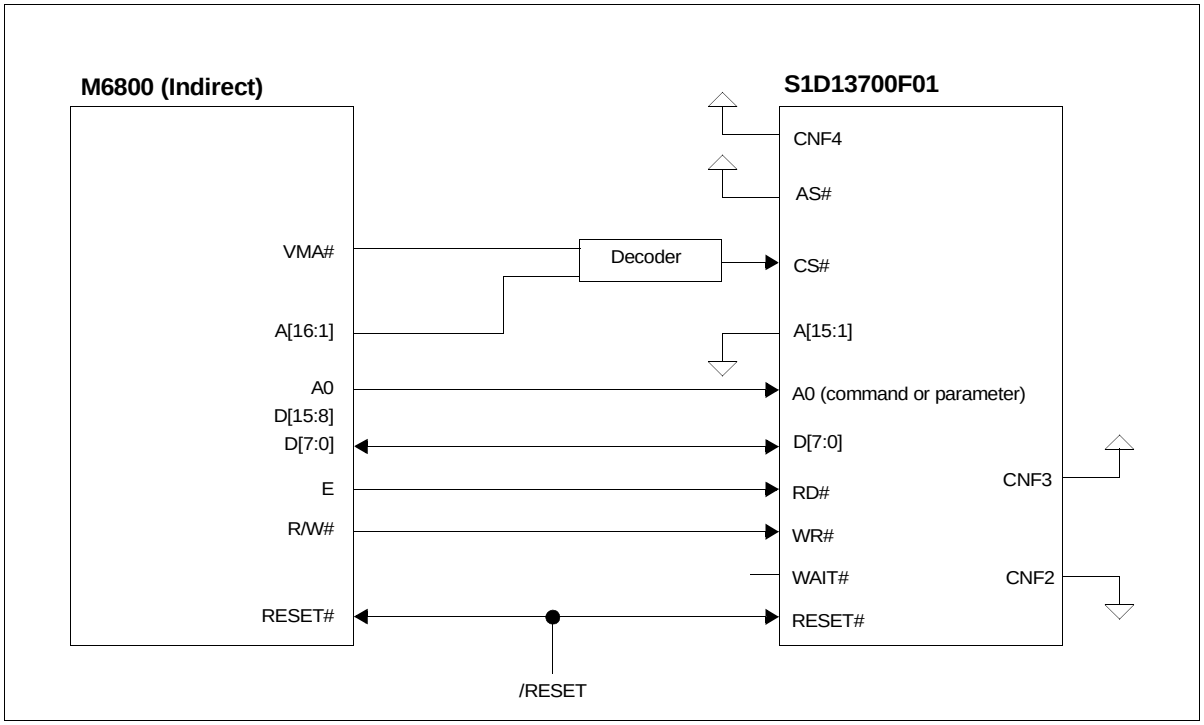


Figure 3-5 Indirect M6800 to S1D13700F01 Interface Example

4 Functional Block Diagram

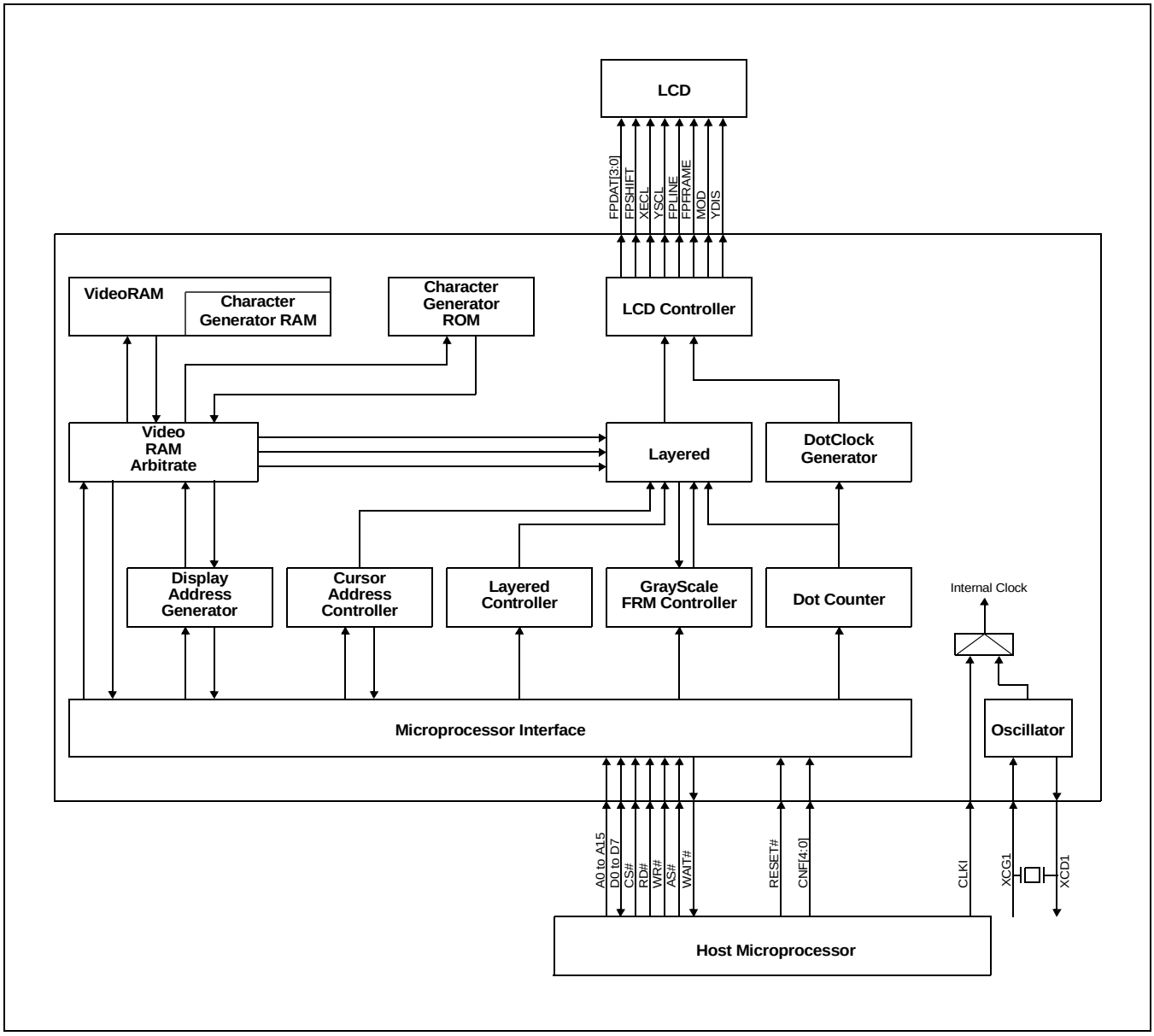


Figure 4-1 Functional Block Diagram

5 Pins

5.1 Pinout Diagram

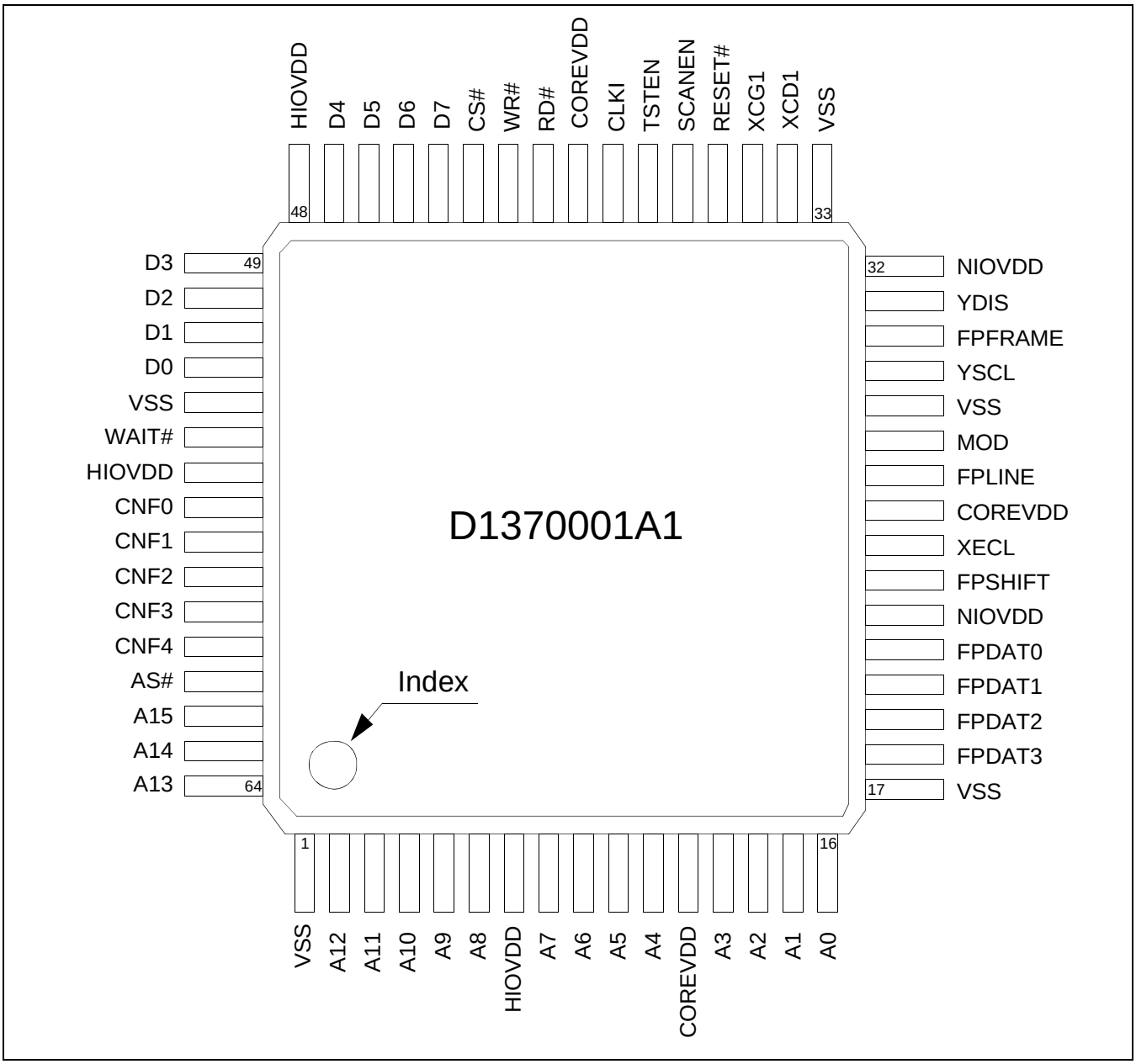


Figure 5-1 Pinout Diagram (TQFP13 - 64 pin)

5.2 Pin Descriptions

Key:

Pin Types

I	=	Input
O	=	Output
IO	=	Bi-Directional (Input/Output)
P	=	Power pin

RESET# States

Z	=	High Impedance (Hi-Z)
L	=	Low level output
H	=	High level output
0	=	Pull-down control on input
1	=	Pull-up control on input

Table 5-1: Cell Descriptions

Item	Description
SI	CMOS level Schmitt input
CI	CMOS input
CID1	CMOS input with internal pull-down resistor (typical value of 60kΩ@5.0V)
CB2	CMOS IO buffer (6mA/-6mA@3.3V, 8mA/-8mA@5.0V)
OB2T	Output buffer (6mA/-6mA@3.3V) with Test
LIN	TTL transparent input
LOT	TTL transparent output
T1	Test mode control input with pull-down resistor (typical value of 50 kΩ@3.3V)
HTB2T	Tri-state output buffer (6mA/-6mA@3.3V)

5.2.1 Host Interface

Many of the host interface pins have different functions depending on the selection of the host bus interface (see configuration of CNF[4:2] pins in Table 5-6: “Summary of Configuration Options,” on page 20). For a summary of host interface pins, see Table 5-7: “Host Interface Pin Mapping,” on page 21.

Table 5-2 Host Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	Power	RESET# State	Description
A[15:1]	I	62-64, 2-6, 8-11, 13-15	CI	HIOVDD	Z	System Address pins 15-1. • For Direct addressing mode, these pins are used for the system address bits 15-1. • For Indirect addressing mode, these pins must be connected to ground (VSS).
A0	I	16	CI	HIOVDD	Z	System Address pin 0. • For Direct addressing mode, this pin is used for system address bit 0. • For Indirect addressing mode, this pin in conjunction with RD# and WR# determines the type of data present on the data bus.
D[7:0]	IO	44-47, 49-52	CB2	HIOVDD	Z	System data bus pins 7-0. These tristate input/output data pins must be connected to the microprocessor data bus.
CNF[1:0]	I	57, 56	SI	HIOVDD	Z	These input pins are used for configuration of the FPSHIFT clock cycle time and must be connected to either HIOVDD or VSS. For further information, see Section 5.3, “Summary of Configuration Options” on page 20.
CNF[3:2]	I	59, 58	SI	HIOVDD	Z	These input pins select the host bus interface (microprocessor interface) and must be connected to either HIOVDD or VSS. The S1D13700F01 supports Generic processors (such as the 8085 and Z80®), the MC68K family of processors (such as the 68000) and the M6800 family of processors (such as the 6800). For further information, see Section 5.3, “Summary of Configuration Options” on page 20.
CNF4	I	60	SI	HIOVDD	Z	This input pin selects the microprocessor addressing mode and must be connected to either HIOVDD or VSS. The S1D13700F01 supports both Direct and Indirect addressing modes. For further information, see Section 5.3, “Summary of Configuration Options” on page 20.
RD#	I	41	SI	HIOVDD	Z	This input pin has multiple functions. • When the Generic host bus interface is selected, this pin is the active-LOW read strobe (RD#). The S1D13700F01 data output buffers are enabled when this signal is low. • When the M6800 host bus interface is selected, this pin is the active-high enable clock (E). Data is read from or written to the S1D13700F01 when this clock goes high. • When the MC68K host bus interface is selected, this pin is the active-low lower data strobe (LDS#). Data is read from or written to the S1D13700F01 when this signal goes low.

Table 5-2 Host Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	Power	RESET# State	Description
WR#	I	42	SI	HIOVDD	Z	This input pin has multiple functions. • When the Generic host bus interface is selected, this signal is the active-low write strobe (WR#). The bus data is latched on the rising edge of this signal. • When the M6800 host bus interface is selected, this signal is the read/write control signal (R/W#). Data is read from the S1D13700F01 if this signal is high, and written to the S1D13700F01 if it is low. • When the MC68K host bus interface is selected, this signal is the read/write control signal (RD/WR#). Data is read from the S1D13700F01 if this signal is high, and written to the S1D13700F01 if it is low.
CS#	I	43	SI	HIOVDD	Z	Chip select. This active-low input enables the S1D13700F01. It is usually connected to the output of an address decoder device that maps the S1D13700F01 into the memory space of the controlling microprocessor.
WAIT#	O	54	HTB2T	HIOVDD	Z	This output pin has multiple functions. • When the Generic host bus interface is selected, this pin is WAIT#. During a data transfer, WAIT# is driven active-low to force the system to insert wait states. It is driven inactive to indicate the completion of a data transfer. WAIT# is released to a high impedance state after the data transfer is complete. For indirect addressing mode, the WAIT# pin can be used to handshake with the Host. • When the MC68K host bus interface is selected, this pin is DTACK#. During a data transfer, DTACK# is driven active-high to force the system to insert wait states. It is driven inactive to indicate the completion of a data transfer. DTACK# is released to a high impedance state after the data transfer is complete. For indirect addressing mode, the DTACK# pin can be used to handshake with the Host. • When the M6800 host bus interface is selected, this pin must be left unconnected and floating.
AS#	I	61	CI	HIOVDD	Z	This input pin has multiple functions. • When the Generic host bus interface is selected, this pin must be connected to VDD (pulled high). • When the MC68K host bus interface is selected, this pin is the address strobe (AS#). • When the M6800 host bus interface is selected, this pin must be connected to VDD (pulled high).
RESET#	I	36	SI	HIOVDD	Z	This active-low input performs a hardware reset of the S1D13700F01 which sets all internal registers to their default states and forces all signals to their inactive states. Note: Do not trigger a RESET# when the supply voltage is lowered.
SCANEN	I	37	CID1	HIOVDD	0	Reserved This pin must be connected to ground (VSS).
TSTEN	I	38	T1	HIOVDD	0	Reserved This pin must be connected to ground (VSS).

5.2.2 LCD Interface

In order to provide effective low-power drive for LCD matrixes, the S1D13700F01 can directly control both the X and Y-drivers using an enable chain.

Table 5-3 LCD Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	Power	RESET# State	Description
FPDAT[3:0] (XD[3:0])	O	18-21	OB2T	NIOVDD	X	These output pins are the 4-bit X-driver (column drive) data outputs and must be connected to the inputs of the X-driver chips.
FPSHIFT (XSCL)	O	23	OB2T	NIOVDD	X	The falling edge of FPSHIFT latches the data on FPDAT[3:0] into the input shift registers of the X-drivers. To conserve power, this clock is stopped between FPLINE and the start of the following display line.
XECL	O	24	OB2T	NIOVDD	X	The falling edge of XECL triggers the enable chain cascade for the X-drivers. Every 16th clock pulse is output to the next X-driver.
FPLINE (LP)	O	26	OB2T	NIOVDD	X	FPLINE latches the signal in the X-driver shift registers into the output data latches. FPLINE is a falling edge triggered signal, and pulses once every display line. FPLINE must be connected to the Y-driver shift clock on LCD modules.
MOD (WF)	O	27	OB2T	NIOVDD	X	This output pin is the LCD panel backplane bias signal. The MOD period is selected using the SYSTEM SET command.
YSCL	O	29	OB2T	NIOVDD	X	The falling edge of YSCL latches the data on FPFRAME into the input shift registers of the Y-drivers. YSCL is not used with driver ICs which use FPLINE as the Y-driver shift clock.
FPFRAME (YD)	O	30	OB2T	NIOVDD	X	This output pin is the data pulse output for the Y drivers. It is active during the last line of each frame, and is shifted through the Y drivers one by one (by YSCL), to scan the display's common connections.
YDIS	O	31	OB2T	NIOVDD	L	This output pin is the power-down output signal. YDIS is high while the display drive outputs are active. YDIS goes low one or two frames after the power save command is written to the S1D13700F01. All Y-driver outputs are forced to an intermediate level (de-selecting the display segments) to blank the display. In order to implement power-down operation in the LCD unit, the LCD power drive supplies must also be disabled when the display is disabled by YDIS.

5.2.3 Clock Input

Table 5-4 Clock Input Pin Descriptions

Pin Name	Type	Pin #	Cell	Power	RESET# State	Description
XCG1	I	35	LIN	COREVDD	Z	This input pin is the crystal connection for use with the internal oscillator. This pin must be pulled down when using an external clock source (CLKI). For further information on the use of the internal oscillator, see Section 9.3, “Oscillator Circuit” on page 43.
XCD1	O	34	LOT	COREVDD	—	This output pin is the crystal connection for use with the internal oscillator. This pin must be left unconnected when using an external clock source (CLKI). For further information on the use of the internal oscillator, see Section 9.3, “Oscillator Circuit” on page 43.
CLKI	I	39	CI	HIOVDD	Z	This is the external clock input. This pin must be pulled down when using a crystal with the internal oscillator. For further information on clocks, see Section 9, “Clocks” on page 42.

5.2.4 Power And Ground

Table 5-5 Power And Ground Pin Descriptions

Pin Name	Type	Pin #	Cell	Power	RESET# State	Description
HIOVDD	P	55, 48, 7	P	—	—	IO power supply for the Host (MPU) interface, 3.3/5.0 volts.
NIOVDD	P	32, 22	P	—	—	IO power supply for the LCD interface, 3.3/5.0 volts.
COREVDD	P	40, 25, 12	P	—	—	Core power supply, 3.3 volts.
VSS	P	53, 33, 28, 17, 1	P	—	—	Ground for HIOVDD, NIOVDD, and COREVDD

5.3 Summary of Configuration Options

These pins are used for configuration of the chip and must be connected directly to HIOVDD or VSS.

Note
The state of CNF[4:0] can be set at any time before or during operation of the S1D13700F01.

Table 5-6: Summary of Configuration Options

Configuration Input	Configuration State	
	1 (connected to HIOVDD)	**0 (connected to VSS)**
CNF4	Indirect Addressing Mode: 1-bit address bus 8-bit data bus 9 pins are used	DIrect Addressing Mode: 16-bit address bus 8-bit data bus 24 pins are used
CNF[3:2]	Select the host bus interface as follows: **CNF3 CNF2 Host Bus** 0 0 Generic Bus 0 1 Reserved 1 0 M6800 Family Bus Interface 1 1 MC68K Family Bus Interface	
CNF[1:0]	Select the FPSHIFT cycle time (FPSHIFT:Clock Input) as follows: **CNF1 CNF0 FPSHIFT Cycle Time** 0 0 4:1 0 1 8:1 1 0 16:1 1 1 Reserved	

5.4 Host Bus Interface Pin Mapping

Table 5-7: Host Interface Pin Mapping

Pin Name	Generic Direct	Generic Indirect	MC68K Direct	MC68K Indirect	M6800 Direct	M6800 Indirect
A[15:1]	A[15:1]	Connected to VSS	A[15:1]	Connected to VSS	Not supported	Connected to VSS
A0	A0	A0	A0	A0		A0
D[7:0]	D[7:0]	D[7:0]	D[7:0]	D[7:0]		D[7:0]
CS#	CS#	CS#	External Decode	External Decode		External Decode
AS#	Connected to HIOVDD	Connected to HIOVDD	AS#	AS#		Connected to HIOVDD
RD#	RD#	RD#	LDS#	LDS#		E
WR#	WR#	WR#	RD/WR#	RD/WR#		R/W#
WAIT#	WAIT# or Unconnected		DTACK# or Unconnected			Unconnected
RESET#	RESET#	RESET#	RESET#	RESET#		RESET#
CNF4	Connected to VSS	Connected to HIOVDD	Connected to VSS	Connected to HIOVDD		Connected to HIOVDD
CNF3	Connected to VSS	Connected to VSS	Connected to HIOVDD	Connected to HIOVDD		Connected to HIOVDD
CNF2	Connected to VSS	Connected to VSS	Connected to HIOVDD	Connected to HIOVDD		Connected to VSS
CNF[1:0]	See Note	See Note	See Note	See Note		See Note

Note

CNF[1:0] are used to configure the FPSHIFT cycle time and must be set according to the requirements of the specific implementation.

6 D.C. Characteristics

Table 6-1 Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
CORE V_{DD}	Supply Voltage	V_{SS} - 0.3 to 4.0	V
IO V_{DD}	Supply Voltage	V_{SS} - 0.3 to 7.0	V
V_{IN}	Input Voltage	V_{SS} - 0.3 to IO V_{DD} + 0.5	V
V_{OUT}	Output Voltage	V_{SS} - 0.3 to IO V_{DD} + 0.5	V
T_{STG}	Storage Temperature	-65 to 150	° C
T_{SOL}	Solder Temperature/Time	260 for 10 sec. max at lead	° C

Table 6-2 Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
Core V_{DD}	Supply Voltage	V_{SS} = 0 V	3.0	3.3	3.6	V
HIO V_{DD}	Host Bus IO Supply Voltage	V_{SS} = 0 V	3.0	3.3	3.6	V
			4.5	5.0	5.5	V
NIO V_{DD}	Panel IO Supply Voltage	V_{SS} = 0 V	3.0	3.3	3.6	V
			4.5	5.0	5.5	V
HIO V_{IN}	Host Input Voltage		V_{SS}		HIO V_{DD}	V
NIO V_{IN}	Non-Host Input Voltage		V_{SS}		NIO V_{DD}	V
T_{OPR}	Operating Temperature		-40	25	85	° C

Table 6-3 Electrical Characteristics for VDD = 3.3V typical

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{QH}	Core Quiescent Current	Power save mode enabled	—	—	35	µA
	IO Quiescent Current	Power save mode enabled	—	—	30	µA
I_{LZ}	Input Leakage Current		-1	—	1	µA
I_{OZ}	Output Leakage Current		-1	—	1	µA
V_{OH}	High Level Output Voltage	VDD = min. I_{OH} = -6mA	V_{DD}-0.4	—	—	V
V_{OL}	Low Level Output Voltage	VDD = min. I_{OL} = 6mA	—	—	0.4	V
V_{IH1}	High Level Input Voltage	LVTTL Level, V_{DD} = max	2.0	—	—	V
V_{IL1}	Low Level Input Voltage	LVTTL Level, V_{DD} = min.	—	—	0.8	V
V_{T+}	High Level Input Voltage	LVTTL Schmitt	1.1	—	2.4	V
V_{T-}	Low Level Input Voltage	LVTTL Schmitt	0.6	—	1.8	V
V_{H1}	Hysteresis Voltage	LVTTL Schmitt	0.1	—	—	V
R_{PD}	Pull Down Resistance	$V_I = V_{DD}$	20	50	120	kΩ

Table 6-4 Electrical Characteristics for VDD = 5.0V typical

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{QH}	Core Quiescent Current	Power save mode enabled	—	—	35	µA
	IO Quiescent Current	Power save mode enabled	—	—	30	µA
I_{LZ}	Input Leakage Current		-1	—	1	µA
I_{OZ}	Output Leakage Current		-1	—	1	µA
V_{OH}	High Level Output Voltage	VDD = min. I_{OH} = -8mA	V_{DD}-0.4	—	—	V
V_{OL}	Low Level Output Voltage	VDD = min. I_{OL} = 8mA	—	—	0.4	V
V_{IH}	High Level Input Voltage	CMOS Level, V_{DD} = max	3.5	—	—	V
V_{IL}	Low Level Input Voltage	CMOS Level, V_{DD} = min.	—	—	1.0	V
V_{T+}	High Level Input Voltage	CMOS Schmitt	2.0	—	4.0	V
V_{T-}	Low Level Input Voltage	CMOS Schmitt	0.8	—	3.1	V
V_H	Hysteresis Voltage	CMOS Schmitt	0.3	—	—	V
R_{PD}	Pull Down Resistance	$V_I = V_{DD}$	30	60	144	kΩ

The following electrical characteristics from Table 6-3 “Electrical Characteristics for VDD = 3.3V typical,” on page 22 and Table 6-4 “Electrical Characteristics for VDD = 5.0V typical,” on page 23 apply to the following cell types.

Table 6-5 Cell Type Reference

Electrical Characteristic	Cell Type
V_{OH} / V_{OL}	OB2T CB2 HTB2T
V_{IH} / V_{IL}	CI CID1 CB2
V_{T+} / V_{T-}	SI
V_H	SI
R_{PD}	CID1

7 A.C. Characteristics

Conditions: Core V_{DD} = 3.3V ± 10%
IO V_{DD} = 3.3V ± 10% or 5.0V ± 10%

T_{OPR} = -40° C to 85° C
T_{rise} and T_{fall} for all inputs must be ≤ 5 nsec (10% ~ 90%)
C_L = 30pF (Bus/MPU Interface)
C_L = 30pF (LCD Panel Interface)

Note
C_L includes a maximum pin capacitance of 5pF.

7.1 Clock Timing

7.1.1 Input Clock

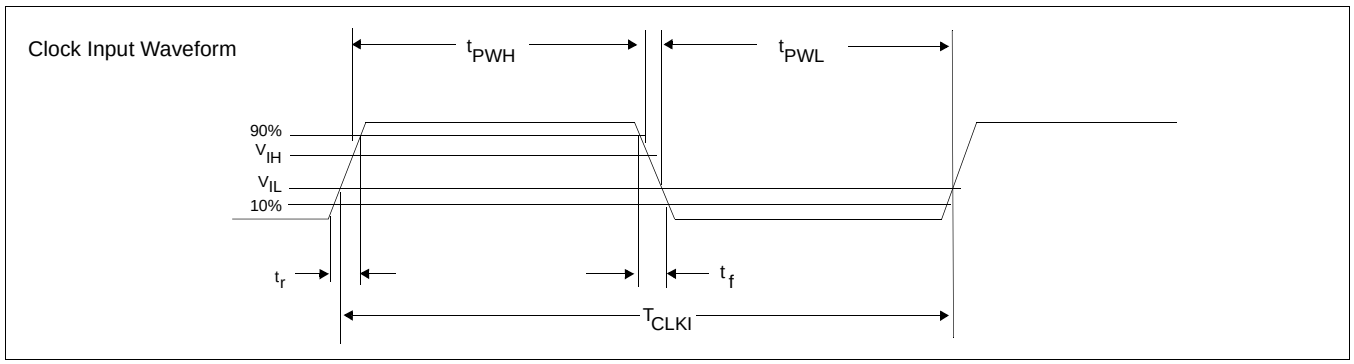


Figure 7-1 Clock Input Requirements

Table 7-1 Clock Input Requirements

Symbol	Parameter	3.0V		5.0V		Units
		Min	Max	Min	Max	
f_{CLKI}	Input Clock Frequency (CLKI)	—	60	—	60	MHz
T_{CLKI}	Input Clock period (CLKI)	$1/f_{OSC}$	—	$1/f_{OSC}$	—	ns
t_{PWH}	Input Clock Pulse Width High (CLKI)	$0.4T_{CLKI}$	—	$0.4T_{CLKI}$	—	ns
t_{PWL}	Input Clock Pulse Width Low (CLKI)	$0.4T_{CLKI}$	—	$0.4T_{CLKI}$	—	ns
t_f	Input Clock Fall Time (10% - 90%)	—	2	—	2	ns
t_r	Input Clock Rise Time (10% - 90%)	—	2	—	2	ns

Note
Maximum internal requirements for clocks derived from CLKI must be considered when determining the frequency of CLKI. For further details on internal clocks, see Section 9, “Clocks” on page 42.

7.2 Reset Timing

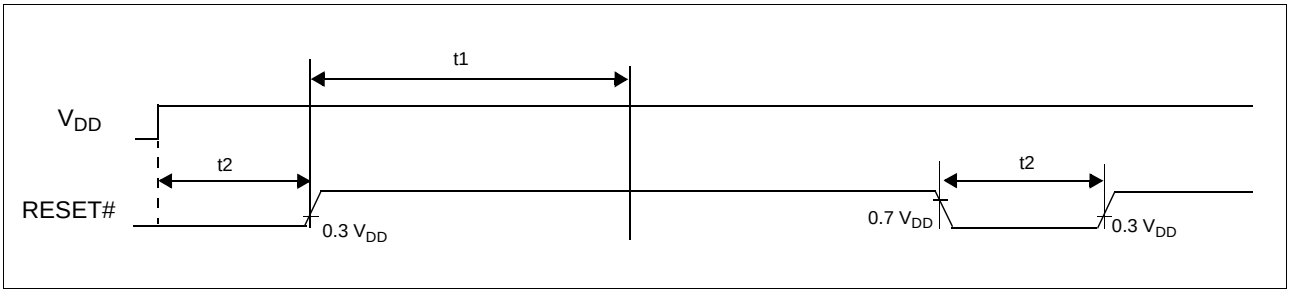


Figure 7-2 Reset Timing

Table 7-2 Reset Timing

Symbol	Parameter	Min	Max	Units
t1	Oscillator stable delay (Note 1)	3	—	ms
t2	Reset pulse duration (Note 2)	1	—	ms

1. A delay is required following the rising edges of both RESET# and VDD to allow for system stabilization. This delay allows the clock used by the internal oscillator circuit to become stable before use. The LCDC must not be accessed before the oscillation circuit is stable.

2. The S1D13700F01 requires a reset pulse of at least 1 ms after power-on in order to re-initialize its internal state. For maximum reliability, it is not recommended to apply a DC voltage to the LCD panel while the S1D13700F01 is reset. Turn off the LCD power supplies for at least one frame period after the start of the reset pulse.

   Note that during the reset period the S1D13700F01 cannot receive commands. Commands to initialize the internal registers should be issued soon after a reset. During reset, the LCD drive signals FPDAT, FPLINE and FR are halted.

7.3 CPU Interface Timing

7.3.1 Generic Bus Direct/Indirect Interface with WAIT# Timing

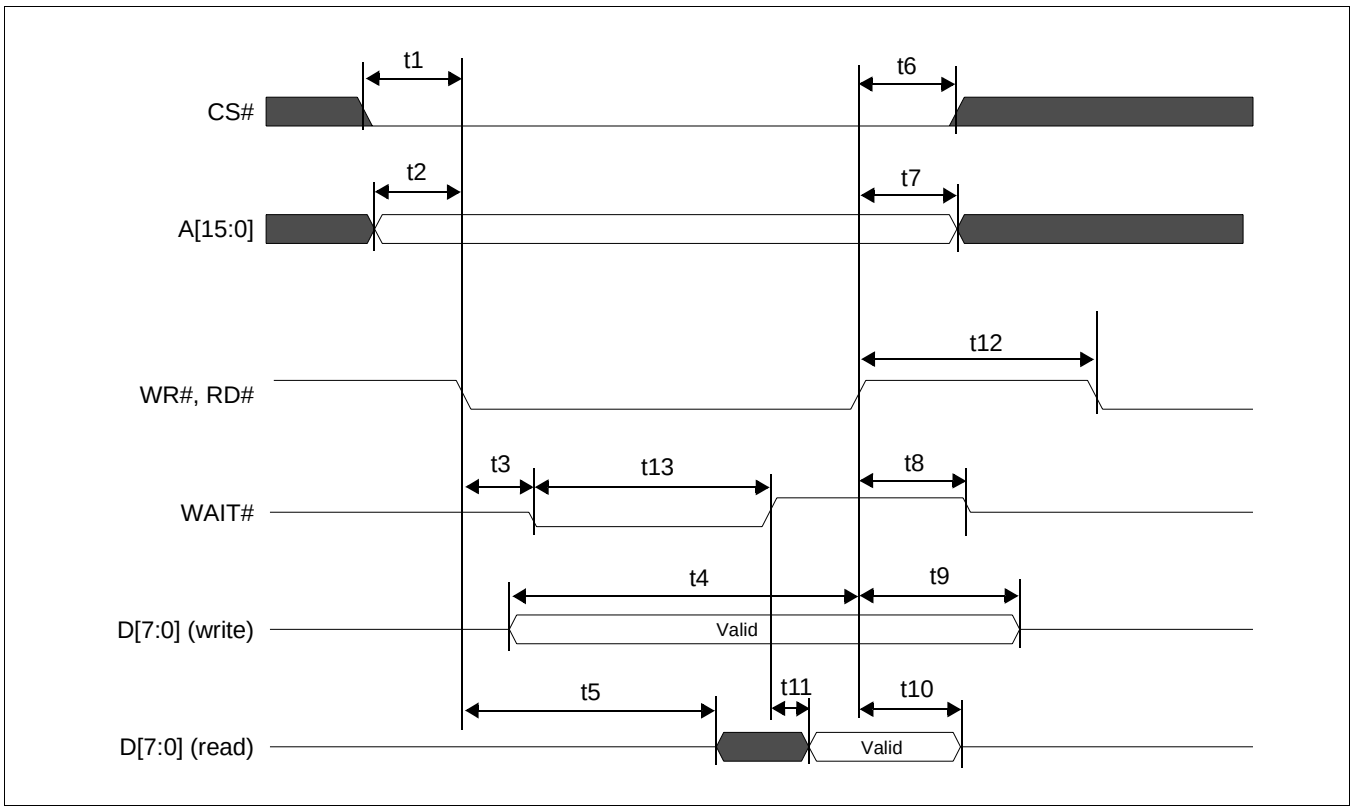


Figure 7-3 Generic Bus Direct/Indirect Interface with WAIT# Timing

Table 7-3 Generic Bus Direct/Indirect Interface with WAIT# Timing

Symbol	Parameter	3.3 Volt		5.0 Volt		Units
		Min	Max	Min	Max	
t1	CS# setup time	5	—	5	—	ns
t2	A[15:0] setup time	5	—	5	—	ns
t3	WR#, RD# falling edge to WAIT# driven low	2	15	2	15	ns
t4	D[7:0] setup time to WR# rising edge (write cycle)	Note 2	—	Note 2	—	ns
t5	RD# falling edge to D[7:0] driven (read cycle)	3	—	3	—	ns
t6	CS# hold time	7	—	7	—	ns
t7	A[15:0] hold time	7	—	7	—	ns
t8	RD#, WR# rising edge to WAIT# high impedance	2	10	2	10	ns
t9	D[7:0] hold time from WR# rising edge (write cycle)	5	—	5	—	ns
t10	D[7:0] hold time from RD# rising edge (read cycle)	3	14	3	14	ns
t11	WAIT# rising edge to valid Data	—	Note 3	—	Note 3	ns
t12	RD#, WR# pulse inactive time	Note 4	—	Note 4	—	ns
t13	WAIT# pulse active time	—	Note 5	—	Note 5	ns

1. Ts = System clock period
2. t4min = 2Ts + 5
3. t11max = 1Ts + 5 (for 3.3V)
   = 1Ts + 7 (for 5.0V)
4. t12min = 1Ts (for a read cycle followed by a read or write cycle)
   = 2Ts + 2 (for a write cycle followed by a write cycle)
   = 5Ts + 2 (for a write cycle followed by a read cycle)
5. t13max = 4Ts + 2

7.3.2 Generic Bus Direct/Indirect Interface without WAIT# Timing

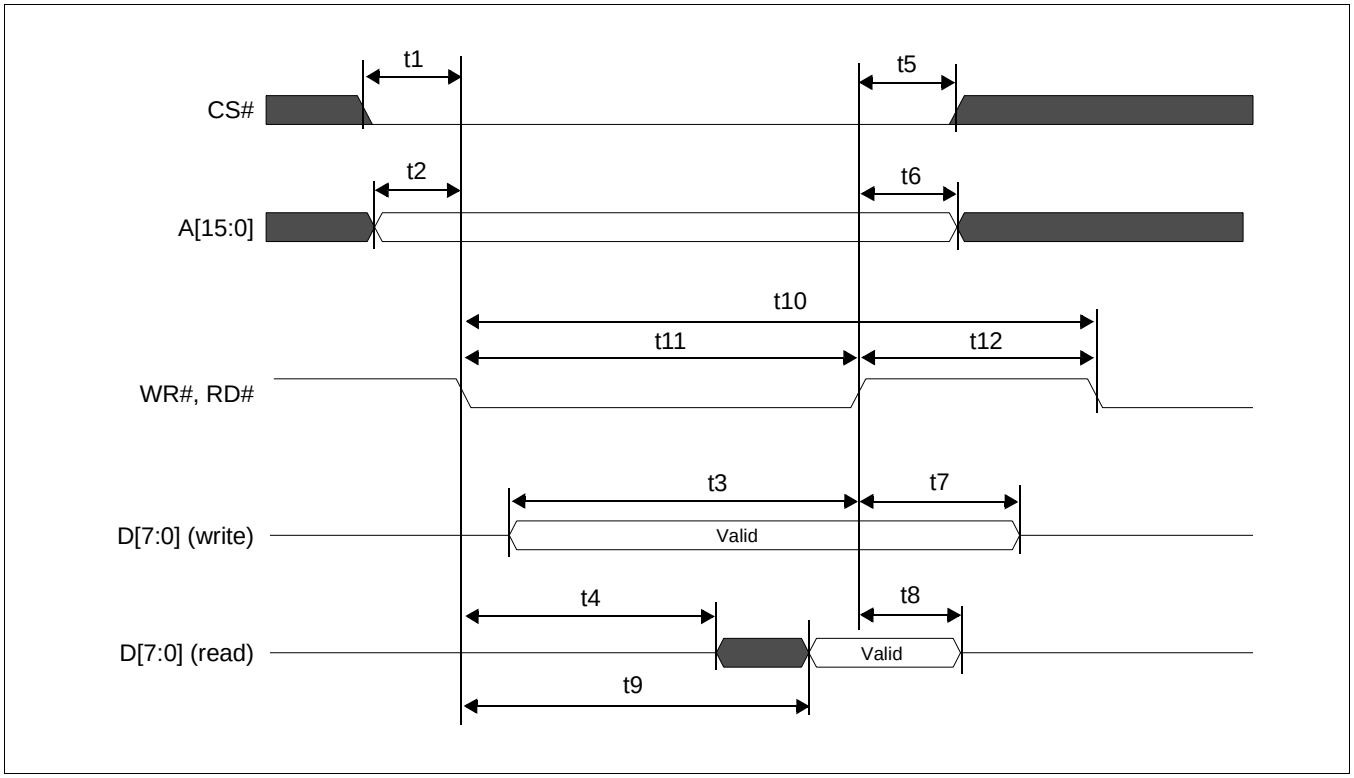


Figure 7-4 Generic Bus Direct/Indirect Interface without WAIT# Timing

Table 7-4 Generic Bus Direct/Indirect Interface without WAIT# Timing

Symbol	Parameter	3.3 Volt		5.0 Volt		Units
		Min	Max	Min	Max	
t1	CS# setup time	5	—	5	—	ns
t2	A[15:0] setup time	5	—	5	—	ns
t3	D[7:0] setup time to WR# rising edge (write cycle)	Note 2	—	Note 2	—	ns
t4	RD# falling edge to D[7:0] driven (read cycle)	3	—	3	—	ns
t5	CS# hold time	7	—	7	—	ns
t6	A[15:0] hold time	7	—	7	—	ns
t7	D[7:0] hold time from WR# rising edge (write cycle)	5	—	5	—	ns
t8	D[7:0] hold time from RD# rising edge (read cycle)	3	14	3	14	ns
t9	RD# falling edge to valid Data (read cycle)	—	Note 3	—	Note 3	ns
t10	RD#, WR# cycle time	Note 4	—	Note 4	—	ns
t11	RD#, WR# pulse active time	5	—	5	—	Ts
t12	RD#, WR# pulse inactive time	Note 5	—	Note 5	—	ns

1. Ts = System clock period
2. t3min = 2Ts + 5
3. t9max = 4Ts + 18 (for 3.3V)
   = 4Ts + 20 (for 5.0V)
4. t10min = 6Ts (for a read cycle followed by a read or write cycle)
   = 7Ts + 2 (for a write cycle followed by a write cycle)
   = 10Ts + 2 (for a write cycle followed by a read cycle)
5. t12min = 1Ts (for a read cycle followed by a read or write cycle)
   = 2Ts + 2 (for a write cycle followed by a write cycle)
   = 5Ts + 2 (for a write cycle followed by a read cycle)

7.3.3 MC68K Family Bus Direct/Indirect Interface with DTACK# Timing

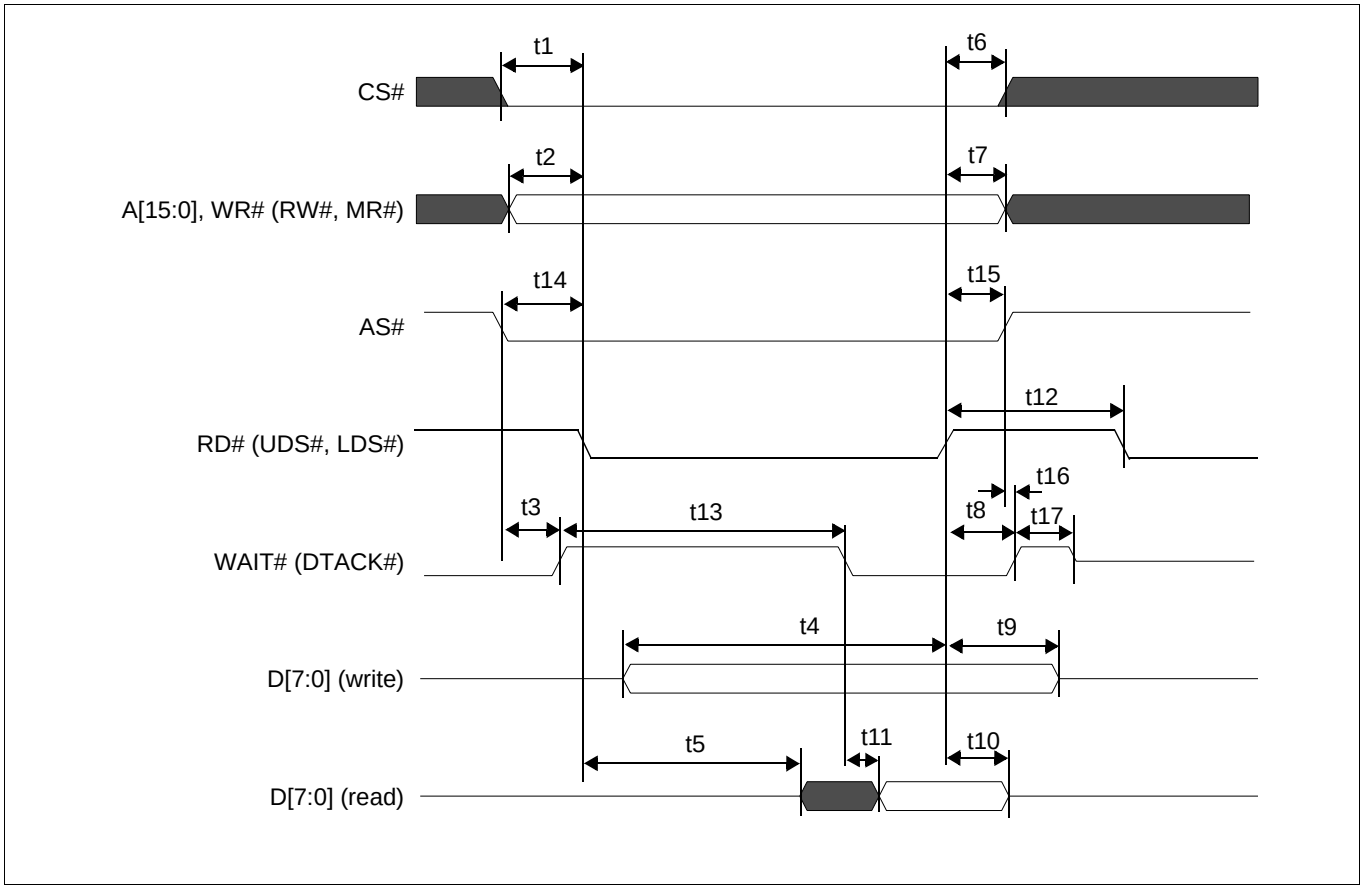


Figure 7-5 MC68K Family Bus Direct/Indirect Interface with DTACK# Timing

Table 7-5 MC68K Family Bus Direct/Indirect Interface with DTACK# Timing

Symbol	Parameter	3.3 Volt		5.0 Volt		Units
		Min	Max	Min	Max	
t1	CS# setup time	5	—	5	—	ns
t2	A[15:0] setup time	5	—	5	—	ns
t3	AS# falling edge to DTACK# driven	2	15	2	15	ns
t4	D[7:0] setup time to RD# rising edge (write cycle)	Note 2	—	Note 2	—	ns
t5	RD# falling edge to D[7:0] driven (read cycle)	3	—	3	—	ns
t6	CS# hold time	7	—	7	—	ns
t7	A[15:0] hold time	7	—	7	—	ns
t8	RD# rising edge to DTACK# high impedance if Direct interface and in Power Save Mode	2	10	2	10	ns
t9	D[7:0] hold time from RD# rising edge (write cycle)	5	—	5	—	ns
t10	D[7:0] hold time from RD# rising edge (read cycle)	2	55	2	55	ns
t11	DTACK# falling edge to valid Data	—	Note 3	—	Note 3	ns
t12	RD# pulse inactive time	Note 4	—	Note 4	—	ns
t13	DTACK# pulse inactive time from DTACK# driven	—	Note 5	—	Note 5	ns
t14	AS# setup time	0	—	0	—	ns
t15	AS# hold time	0	—	0	—	ns
t16	AS# rising edge to DTACK# high de-asserted if not Direct interface and not in Power Save Mode	—	10	—	10	ns
t17	DTACK# pulse inactive time	0	Note 6	0	Note 6	ns

1. Ts = System clock period
2. t4min = 2Ts + 5
3. t11max = 1Ts + 5 (for 3.3V)
   = 1Ts + 7 (for 5.0V)
4. t12min = 1Ts (for a read cycle followed by a read or write cycle)
   = 2Ts + 2 (for a write cycle followed by a write cycle)
   = 5Ts + 2 (for a write cycle followed by a read cycle)
5. t13max = 4Ts + 2
6. t17max = 1Ts - 15

7.3.4 MC68K Family Bus Direct/Indirect Interface without DTACK# Timing

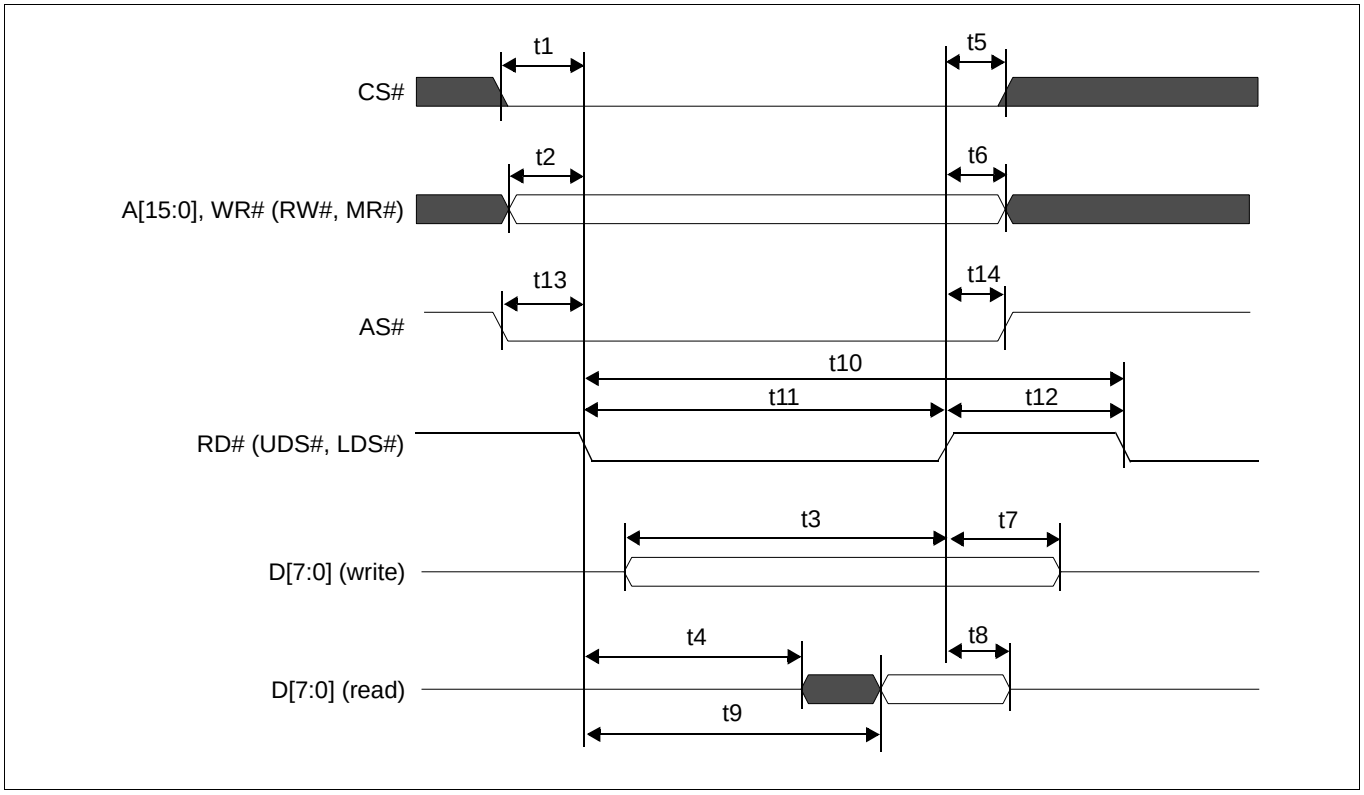


Figure 7-6 MC68K Family Bus Direct/Indirect Interface without DTACK# Timing

Table 7-6 MC68K Family Bus Direct/Indirect Interface without DTACK# Timing

Symbol	Parameter	3.3 Volt		5.0 Volt		Units
		Min	Max	Min	Max	
t1	CS# setup time	5	—	5	—	ns
t2	A[15:0] setup time	5	—	5	—	ns
t3	D[7:0] setup time to RD# rising edge (write cycle)	Note 2	—	Note 2	—	ns
t4	RD# falling edge to D[7:0] driven (read cycle)	3	—	3	—	ns
t5	CS# hold time	7	—	7	—	ns
t6	A[15:0] hold time	7	—	7	—	ns
t7	D[7:0] hold time from RD# rising edge (write cycle)	5	—	5	—	ns
t8	D[7:0] hold time from RD# rising edge (read cycle)	2	55	2	55	ns
t9	RD# falling edge to valid Data	—	Note 3	—	Note 3	ns
t10	RD# cycle time	Note 4	—	Note 4	—	ns
t11	RD# pulse active time	5	—	5	—	Ts
t12	RD# pulse inactive time	Note 5	—	Note 5	—	ns
t13	AS# setup time	0	—	0	—	ns
t14	AS# hold time	0	—	0	—	ns

1. Ts = System clock period
2. t3min = 2Ts + 5
3. t9max = 4Ts + 18 (for 3.3V)
   = 4Ts + 20 (for 5.0V)
4. t10min = 6Ts (for a read cycle followed by a read or write cycle)
   = 7Ts + 2 (for a write cycle followed by a write cycle)
   = 10Ts + 2 (for a write cycle followed by a read cycle)
5. t12min = 1Ts (for a read cycle followed by a read or write cycle)
   = 2Ts + 2 (for a write cycle followed by a write cycle)
   = 5Ts + 2 (for a write cycle followed by a read cycle)

7.3.5 M6800 Family Bus Indirect Interface Timing

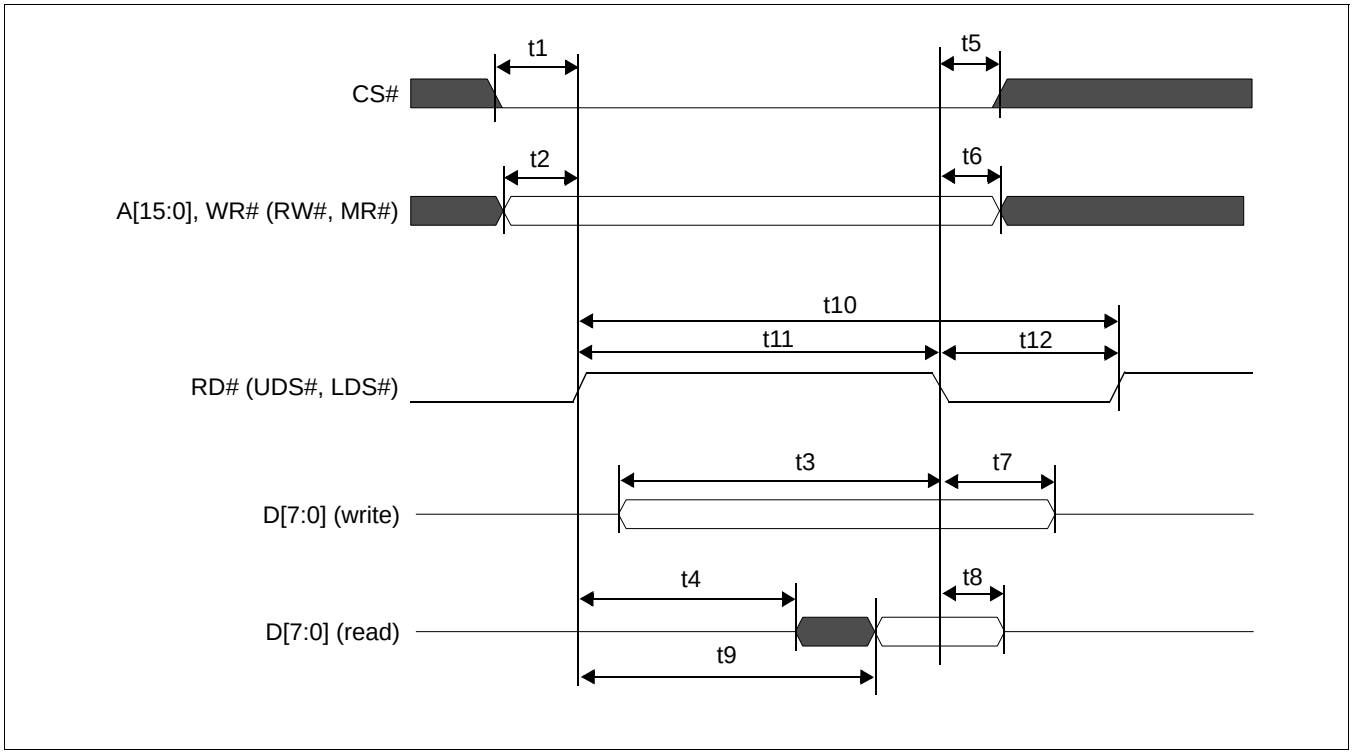


Figure 7-7 M6800 Family Bus Indirect Interface Timing

Table 7-7 M6800 Family Bus Indirect Interface Timing

Symbol	Parameter	3.3 Volt		5.0 Volt		Units
		Min	Max	Min	Max	
t1	CS# setup time	5	—	5	—	ns
t2	A[15:0] setup time	5	—	5	—	ns
t3	D[7:0] setup time to RD# falling edge (write cycle)	Note 2	—	Note 2	—	ns
t4	RD# rising edge to D[7:0] driven (read cycle)	3	—	3	—	ns
t5	CS# hold time	7	—	7	—	ns
t6	A[15:0] hold time	7	—	7	—	ns
t7	D[7:0] hold time from RD# falling edge (write cycle)	5	—	5	—	ns
t8	D[7:0] hold time from RD# falling edge (read cycle)	2	55	2	55	ns
t9	RD# rising edge to valid Data	—	Note 3	—	Note 3	ns
t10	RD# cycle time	Note 4	—	Note 4	—	ns
t11	RD# pulse active time	5	—	5	—	Ts
t12	RD# pulse inactive time	Note 5	—	Note 5	—	ns

1. Ts = System clock period
2. t3min = 2Ts + 5
3. t9max = 4Ts + 18 (for 3.3V)
   = 4Ts + 20 (for 5.0V)
4. t10min = 6Ts (for a read cycle followed by a read or write cycle)
   = 7Ts + 2 (for a write cycle followed by a write cycle)
   = 10Ts + 2 (for a write cycle followed by a read cycle)
5. t12min = 1Ts (for a read cycle followed by a read or write cycle)
   = 2Ts + 2 (for a write cycle followed by a write cycle)
   = 5Ts + 2 (for a write cycle followed by a read cycle)

7.3.6 Display Memory Access Timing for Text Mode

When the microprocessor accesses the display memory, the following timing should be followed. The falling edge of FPLINE can be used as the interrupt signal. Accessing the display memory during times other than the recommended period may result in flickering on the display.

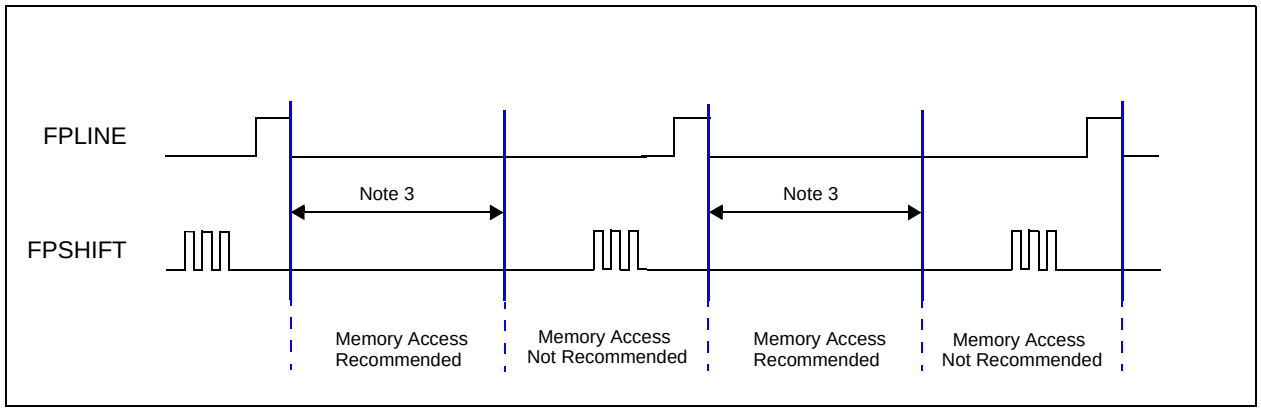


Figure 7-8 Display Memory Access Timing

1. tOSC = 1/fOSC
   = 1 cycle of the oscillator or the CLKI input clock
2. DIV = 2 or 4 or 8
3. Accesses to the display memory are allowed during this time period. It begins from the falling edge of FPLINE and is defined by the following formulas depending on the selected color depth (1, 2, or 4 bpp).
   For 1 bpp, use the following formula: ((TCR + 1) - (CR + 1) - 3) x DIV x 2 x tOSC
   For 2 bpp, use the following formula: ((TCR + 1) - (CR + 1) - 2) x DIV x 2 x tOSC
   For 4 bpp, use the following formula: ((TCR + 1) - (CR + 1) - 1) x DIV x 2 x tOSC

7.4 Power Save Mode/Display Enable Timing

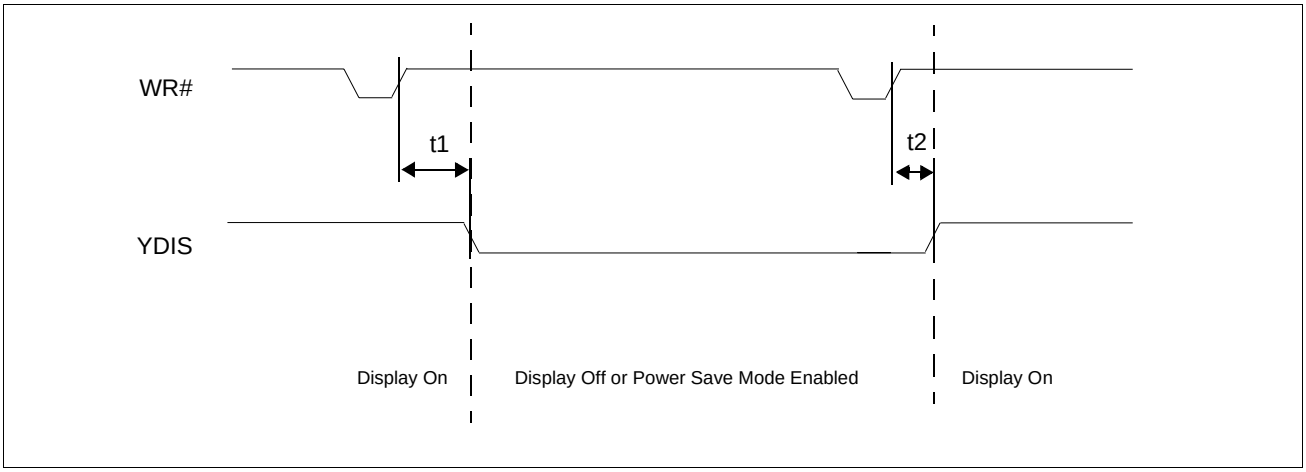


Figure 7-9 Power Save Mode/Display Enable Timing

Table 7-8 Power Save Mode/Display Enable Timing

Symbol	Parameter	3.0 Volt		5.0 Volt		Units
		Min.	Max.	Min.	Max.	
t1a	YDIS falling edge delay for Power Save Mode Enable in Indirect Mode (see Note 2)	—	2	—	2	Frames
t1b	YDIS falling edge delay for Display Off in Indirect Mode (58h)	—	1Ts + 10	—	1Ts + 10	ns
t1c	YDIS falling edge delay for Display Off in Direct Mode (see Note 3)	—	2Ts + 10	—	2Ts + 10	ns
t2	YDIS rising edge delay for Display On (see Note 3)	—	2Ts + 10	—	2Ts + 10	ns

1. Ts = System Clock Period
2. Power Save Mode is controlled by the Power Save Mode Enable bit, REG[08h] bit 0.
3. Display On/Off is controlled by the Display Enable bit, REG[09h] bit 0.

7.5 Display Interface

The timing parameters required to drive a flat panel display are shown below.

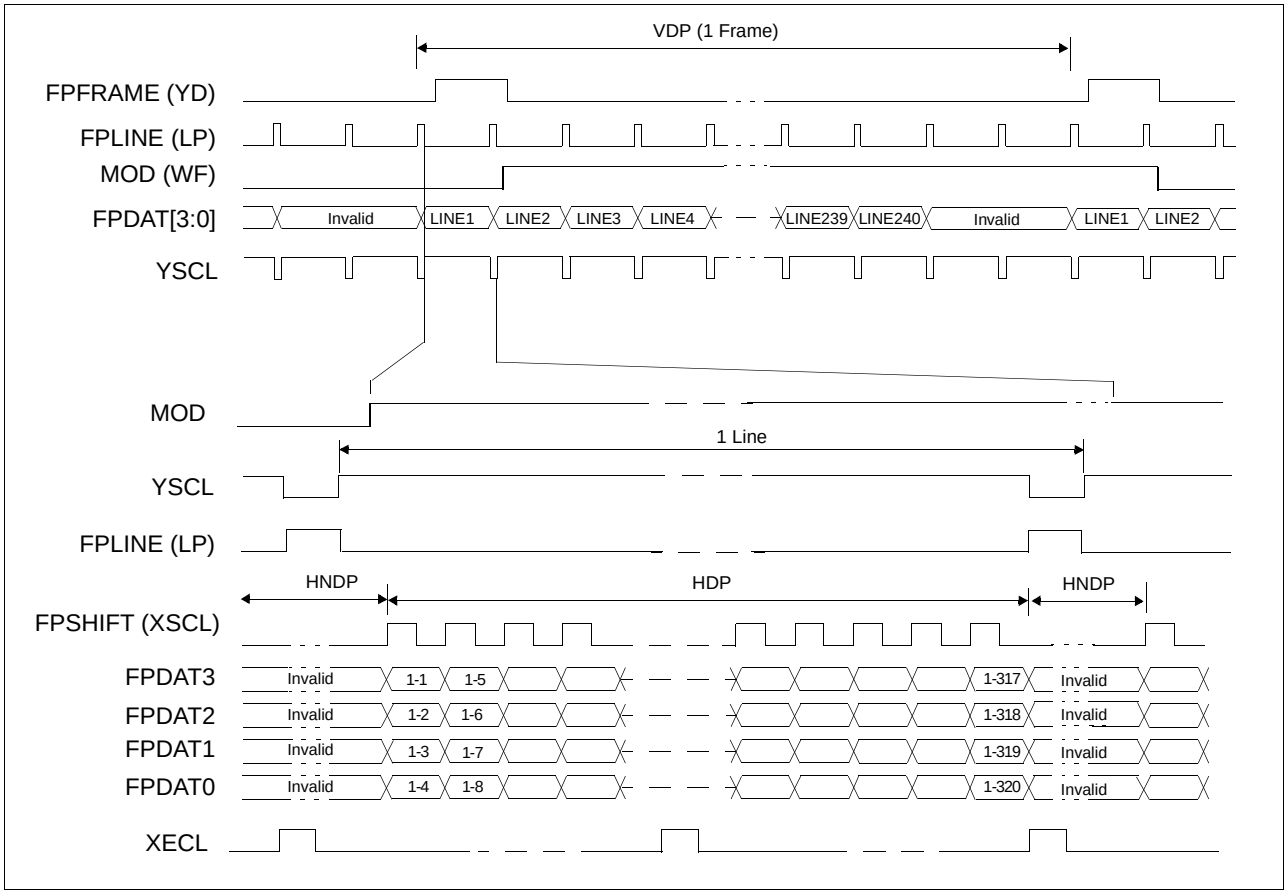


Figure 7-10: Monochrome 4-Bit Panel Timing

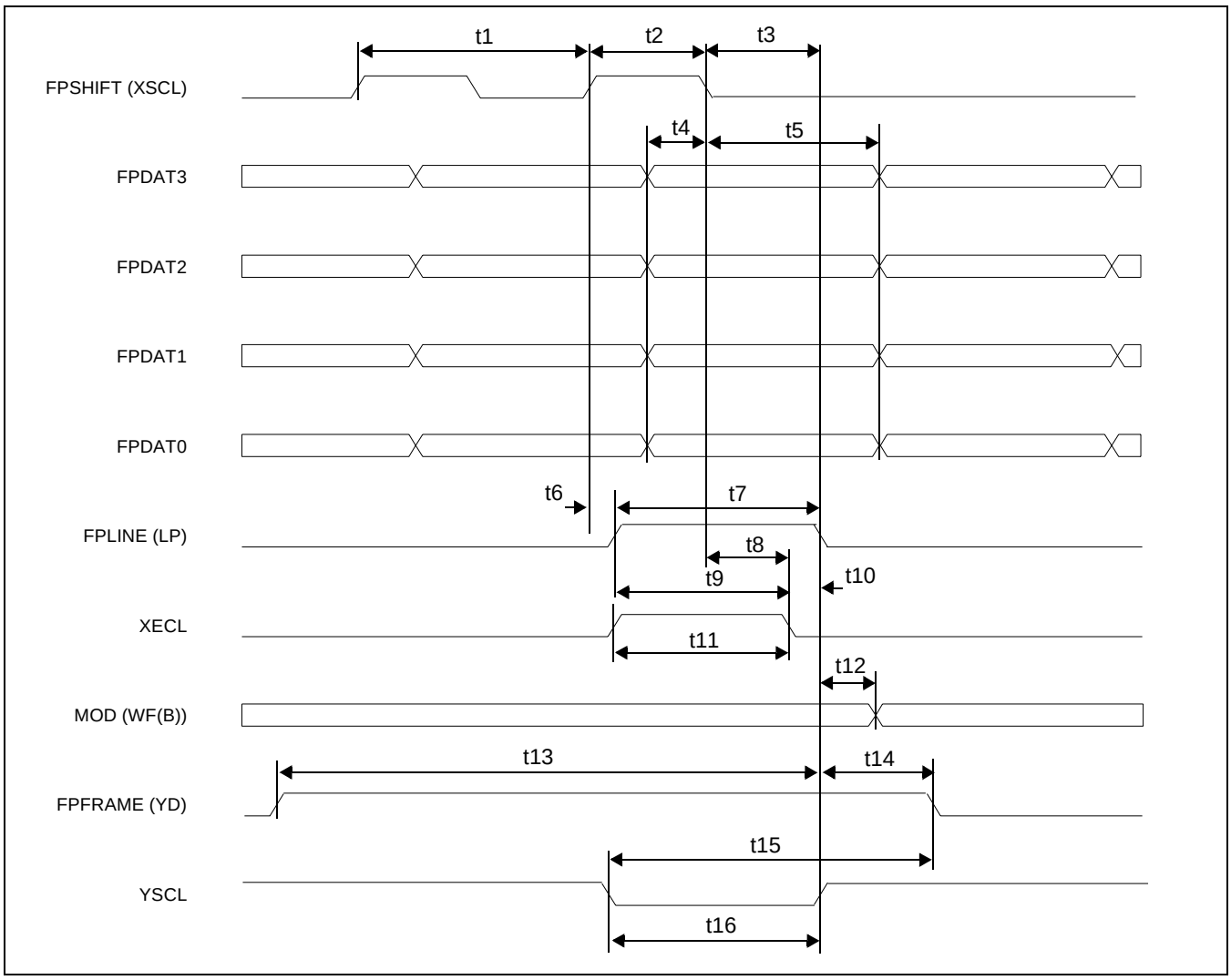

t1
t2
t3
FPSHIFT (XSCL)
t4
t5
FPDAT3
FPDAT2
FPDAT1
FPDAT0
t6
t7
FPLINE (LP)
t8
t9
t10
XECL
t11
t12
MOD (WF(B))
t13
t14
FPFRAME (YD)
t15
YSCL
t16

Table 7-9: Single Monochrome 4-Bit Panel A.C. Timing

Symbol	Parameter	3.3 Volts		5.0 Volts		Units
		Min	Max	Min	Max	
t1	FPSHIFT cycle time	1	—	1	—	Tc (Note 2)
t2	FPSHIFT pulse width	0.5Tc - 5	—	0.5Tc - 4	—	ns
t3	Latch data setup time from FPSHIFT falling edge	0.5Tc - 5	—	0.5Tc - 4	—	ns
t4	FPDAT[3:0] setup to FPSHIFT falling edge	0.5Tc - 5	—	0.5Tc - 4	—	ns
t5	FPDAT[3:0] hold from FPSHIFT falling edge	0.5Tc - 5	—	0.5Tc - 4	—	ns
t6	FPLINE rising edge delay from FPSHIFT rising edge	0	4	0	4	ns
t7	Latch pulse width	Tc - 5	—	Tc - 4	—	ns
t8	XECL falling edge setup time to FPSHIFT falling edge	0.25Tc -5	—	0.25Tc - 4	—	ns
t9	XECL falling edge setup time from FPLINE rising edge	0.75Tc - 5	—	0.75Tc - 4	—	ns
t10	XECL falling edge hold time to FPLINE falling edge	Tc - 8	—	Tc - 8	—	ns
t11	XECL pulse width	0.75Tc - 5	—	0.75Tc - 4	—	ns
t12	Permitted MOD delay time	—	4	—	4	ns
t13	FPLINE falling edge from FPFRAME rising edge	2Tc - 10	—	2Tc - 10	—	ns
t14	FPLINE falling edge to FPFRAME falling edge	2Tc	—	2Tc	—	ns
t15	FPFRAME falling edge hold time from YSCL falling edge	3Tc - 10	—	3Tc - 10	—	ns
t16	YSCL pulse width	Tc - 5	—	Tc - 4	—	ns

1. Ts = System clock period
2. Tc = FPSHIFT cycle time
   = 4Ts when CNF[1:0] = 00
   = 8Ts when CNF[1:0] = 01
   = 16Ts when CNF[1:0] = 10

8 Memory Mapping

The S1D13700F01 includes 32K bytes of embedded SRAM. The memory is used for the display data, the registers and the CGROM.

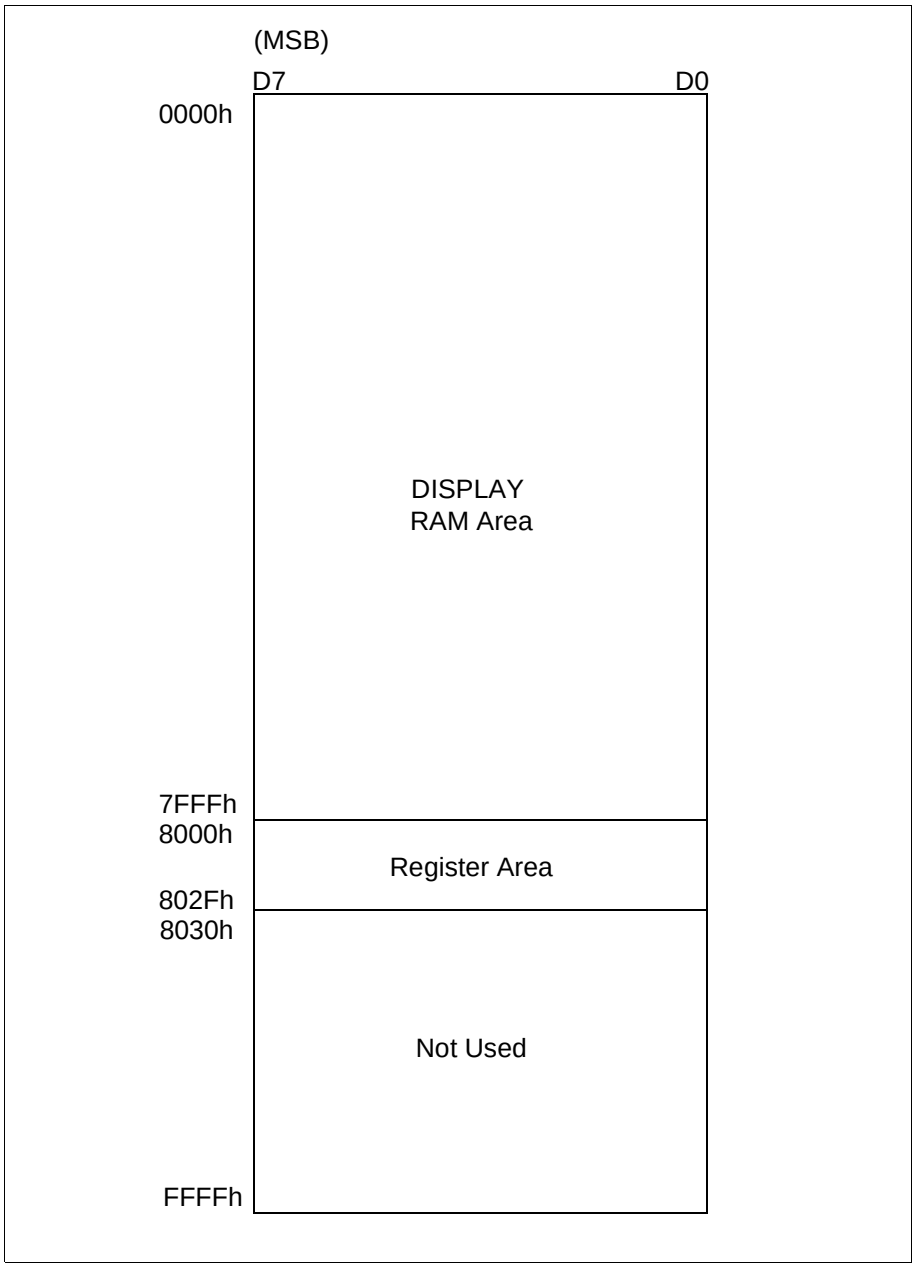


Figure 8-1 S1D13700F01 Memory Mapping

9 Clocks

9.1 Clock Diagram

The following figure shows the clock tree of the S1D13700F01.

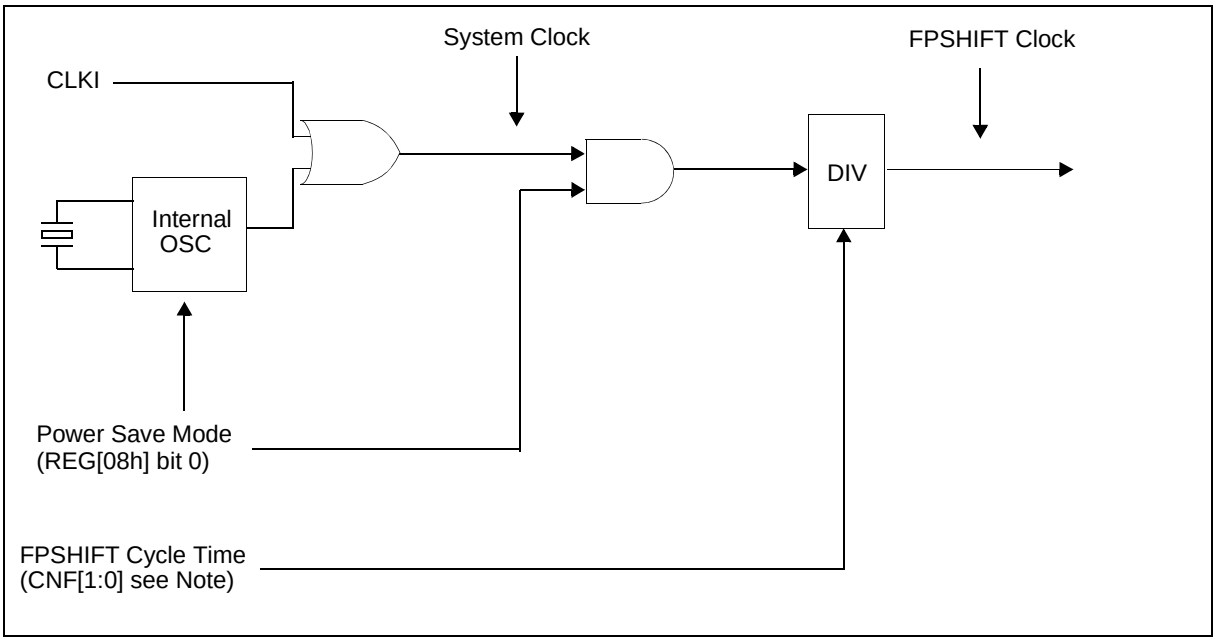


Figure 9-1: Clock Diagram

Note
The FPSHIFT Cycle Time is configured using the CNF[1:0] pins. For further information, see Section 5.3, “Summary of Configuration Options” on page 20.

9.2 Clock Descriptions

9.2.1 System Clock

The maximum frequency of the system clock is 60MHz. The system clock source can be either an external clock source (i.e. oscillator) or the internal oscillator (with external crystal). If an external clock source is used, the crystal input (XCG1) must be pulled down and the crystal output (XCD1) must be left unconnected. If the internal oscillator (with external crystal) is used, the CLKI pin must be pulled down.

9.2.2 FPSHIFT Clock

The FPSHIFT clock is derived from the internal system clock as shown in Figure 9-1: "Clock Diagram," on page 42. The maximum frequency possible for FPSHIFT clock is 15MHz.

9.3 Oscillator Circuit

The S1D13700F01 design incorporates an oscillator circuit. A stable oscillator can be constructed by connecting an AT-cut crystal, two capacitors, and two resistors to XCG1 and XCD1, as shown in the figure below. If the oscillator frequency is increased, Cd and Cg should be decreased proportionally.

Note

The circuit board lines to XCG1 and XCD1 must be as short as possible to prevent wiring capacitance from changing the oscillator frequency or increasing the power consumption.

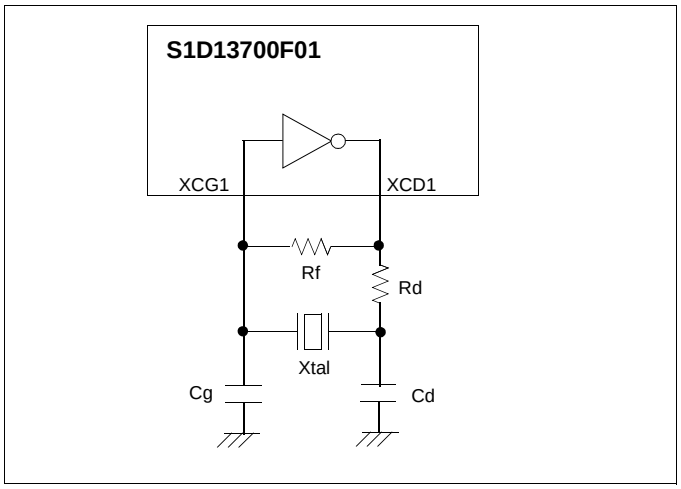


Figure 9-2 Crystal Oscillator

Table 9-1 Crystal Oscillator Circuit Parameters

Symbol	Min	Typ	Max	Units
f_{OSC}	—	40	—	MHz
T_{OSC}	—	$1/f_{OSC}$	—	ns
Rf	—	1	—	MΩ
Rd	—	100	—	Ω
Cg	2	10	18	pF
Cd	3	10	20	pF

10 Registers

10.1 Register Set

The S1D13700F01 registers are listed in the following table.

Table 10-1: S1D13700F01 Register Set

Register	Pg	Register	Pg
LCD Register Descriptions (Offset = 8000h)			
System Control Registers			
REG[00h] Memory Configuration Register	45	REG[01h] Horizontal Character Size Register	49
REG[02h] Vertical Character Size Register	50	REG[03h] Character Bytes Per Row Register	50
REG[04h] Total Character Bytes Per Row Register	50	REG[05h] Frame Height Register	51
REG[06h] Horizontal Address Range Register 0	51	REG[07h] Horizontal Address Range Register 1	51
REG[08h] Power Save Mode Register	52		
Display Control Registers			
REG[09h] Display Enable Register	53	REG[0Ah] Display Attribute Register	53
REG[0Bh] Screen Block 1 Start Address Register 0	55	REG[0Ch] Screen Block 1 Start Address Register 1	55
REG[0Dh] Screen Block 1 Size Register	55	REG[0Eh] Screen Block 2 Start Address Register 0	56
REG[0Fh] Screen Block 2 Start Address Register 1	56	REG[10h] Screen Block 2 Size Register	56
REG[11h] Screen Block 3 Start Address Register 0	57	REG[12h] Screen Block 3 Start Address Register 1	57
REG[13h] Screen Block 4 Start Address Register 0	57	REG[14h] Screen Block 4 Start Address Register 1	57
REG[15h] Cursor Width Register	61	REG[16h] Cursor Height Register	61
REG[17h] Cursor Shift Direction Register	62	REG[18h] Overlay Register	63
REG[19h] Character Generator RAM Start Address Register 0	65	REG[1Ah] Character Generator RAM Start Address Register 1	65
REG[1Bh] Horizontal Pixel Scroll Register	66		
Drawing Control Registers			
REG[1Ch] Cursor Write Register 0	67	REG[1Dh] Cursor Write Register 1	67
REG[1Eh] Cursor Read Register 0	68	REG[1Fh] Cursor Read Register 1	68
GrayScale Register			
REG[20h] Bit-Per-Pixel Select Register	69		

10.2 Register Restrictions

All reserved bits must be set to 0 unless otherwise specified. Writing a value to a reserved bit may produce undefined results. Bits marked as n/a have no hardware effect.

10.3 Register Descriptions

10.3.1 System Control Registers

The following registers initialize the S1D13700F01, set the window sizes, and select the LCD interface format. Incorrect configuration of these registers may cause other commands to operated incorrectly. For an example initialization of the S1D13700F01, see Section 15.1.2, “Initialization Example” on page 104.

SYSTEM SET

The SYSTEM SET command is used to configure the S1D13700F01 for the display used and to exit power save mode **when indirect addressing is used**. The values from REG[00h] through REG[07h] are passed as parameters when the SYSTEM SET command is issued. For further information on the SYSTEM SET command, see Section 11.1.1, “SYSTEM SET” on page 71.

REG[00h] Memory Configuration Register
Address = 8000h Default = 10h Read/Write

n/a		Screen Origin Compensation	Reserved	Panel Drive Select	Character Height	Reserved	Character Generator Select
7	6	5	4	3	2	1	0

Note

When REG[00h] is written to, the S1D13700F01 automatically performs the following functions.

1. Resets the internal timing generator
2. Disables the display
3. When indirect addressing mode is selected, completes and exits power save mode

bit 5 Screen Origin Compensation (IV)

This bit controls Screen Origin Compensation which is used for inverse display and is usually set to 1. A common method of displaying inverted characters is to Exclusive-OR the text layer with the graphics back-ground layer. However when this is done, the inverted characters at the top or left of the screen become difficult to read. This is because the character origin is at the top-left of its bitmap and there are no background pixels either above or to the left of these characters.

This bit causes the S1D13700F01 to offset the text screen against the graphics back layer by one vertical pixel. To shift the text screen horizontally, the horizontal pixel scroll function (REG[1Bh] or the HDOT SCR command for indirect addressing) can be used to shift the text screen 1 to 7 pixels to the right. If both of these functions are enabled, all characters have the appropriate surrounding back-ground pixels to ensure easy reading of the inverted characters.
When this bit = 0, screen origin compensation is done.
When this bit = 1, screen origin compensation is not done.

The following figure shows an example of screen origin compensation and the HDOT SCR command in use.

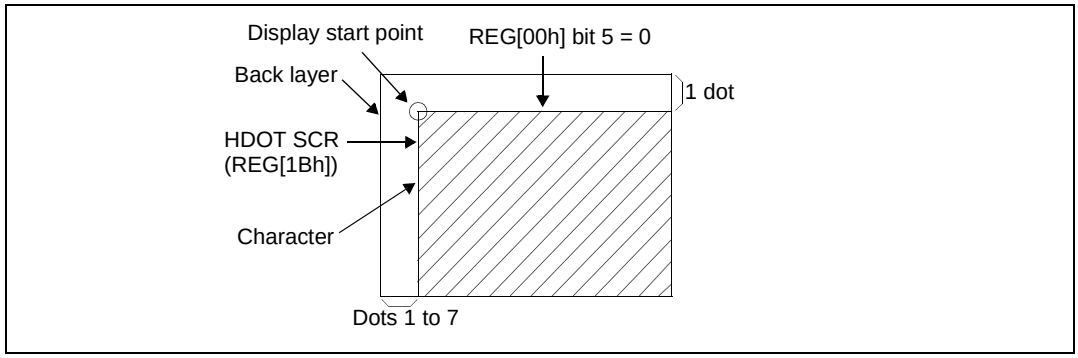


Figure 10-1 Screen Origin Compensation and HDOT SCR Adjustment

bit 4 Reserved

The default value for this bit is 1.

bit 3 Panel Drive Select (W/S)

This bit specifies the LCD panel drive method.
When this bit = 0, a single panel drive is selected.
When this bit = 1, a dual panel drive is selected.

The following diagrams show examples of the possible drive methods.

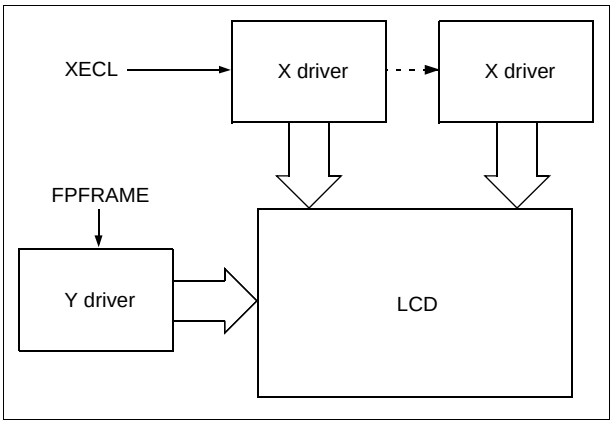


Figure 10-2 Single Drive Panel Display

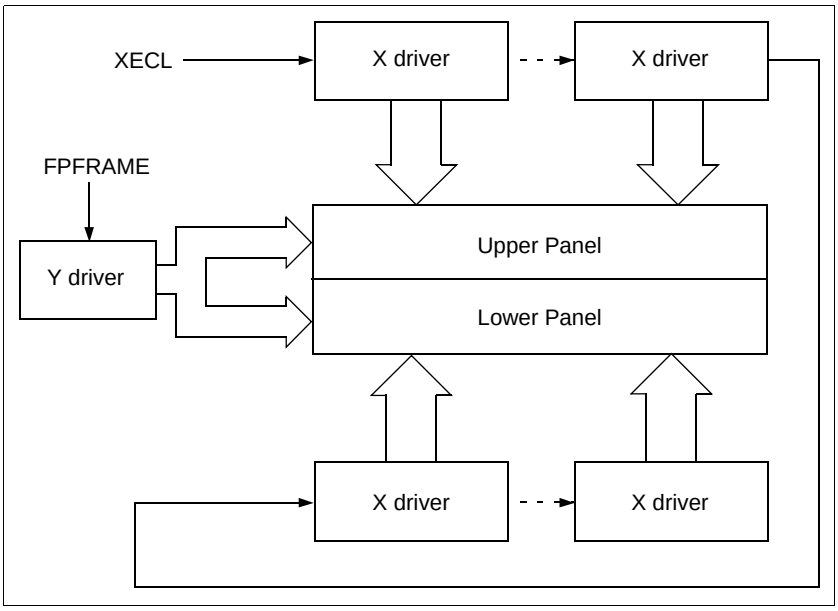


Figure 10-3 Dual Drive Panel Display

The following table summarizes the parameters that must be configured for correct operation of an LCD panel.

Table 10-2 LCD Parameter Summary

Parameter	Single Panel (REG[00h] bit 3 = 0)		Dual Panel (REG[00h] bit 3 = 1)	
	REG[00h] bit 5 = 1 (IV)	**REG[00h] bit 5 = 0 (IV)**	**REG[00h] bit 5 = 1 (IV)**	**REG[00h] bit 5 = 0 (IV)**
C/R	REG[03h] bits 7-0	REG[03h] bits 7-0	REG[03h] bits 7-0	REG[03h] bits 7-0
TC/R	REG[04h] bits 7-0	REG[04h] bits 7-0	REG[04h] bits 7-0	REG[04h] bits 7-0
L/F	REG[05h] bits 7-0	REG[05h] bits 7-0	REG[05h] bits 7-0	REG[05h] bits 7-0
SL1	00h to REG[05h] bits 7-0	00h to REG[05h] bits 7-0 (See Note)	[REG[05h] bits 7-0 + 1] ÷ 2 - 1	[REG[05h] bits 7-0 + 1] ÷ 2 - 1
SL2	00h to REG[05h] bits 7-0	00h to REG[05h] bits 7-0 (See Note)	[REG[05h] bits 7-0 + 1] ÷ 2 - 1	[REG[05h] bits 7-0 + 1] ÷ 2 - 1
SAD1	First screen block (Start Address = REG[0Bh], REG[0Ch])			
SAD2	Second screen block (Start Address = REG[0Eh], REG[0Fh])			
SAD3	Third screen block (Start Address = REG[11h], REG[12h])			
SAD4	Invalid		Fourth screen block (Start Address = REG[13h], REG[14h])	
Cursor movement range	Continuous movement over whole screen		Above-and-below configuration: continuous movement over whole screen	

Note

Screen Origin Compensation shifts the character font down by one pixel row. If the bottom pixel row of the font is at the bottom of the Screen Block, that row disappears when REG[00h] bit 5 = 0. To compensate for the bad visual effect, SL can be increased by one.

bit 2 Character Height (M2)

This bit selects the height of the character bitmaps. It is possible to display characters greater than 16 pixels high by creating a bitmap for each portion of each character and using graphics mode to reposition them.
When this bit = 0, the character height is 8 pixels.
When this bit = 1, the character height is 16 pixels.

bit 1 Reserved

The default value for this bit is 0.

bit 0 Character Generator Select (M0)

This bit determines whether characters are generated by the internal character generator ROM (CGROM) or character generator RAM (CGRAM). The CGROM contains 160, 5x7 pixel characters which are fixed at fabrication. The CGRAM can contain up to 256 user-defined characters which are mapped at the CG Start Address (REG[1Ah] - REG[19h]). However, when the CGROM is used, the CGRAM can only contain up to 64, 8x8 pixel characters.
When this bit = 0, the internal CGROM is selected.
When this bit = 1, the internal CGRAM is selected.

Note

If the CGRAM is used (includes CGRAM1 and CGRAM2), only 1 bpp is supported.

REG[01h] Horizontal Character Size Register
Address = 8001h Default = 00h Read/Write

MOD	n/a			Horizontal Character Size bits 3-0			
7	6	5	4	3	2	1	0

bit 7 MOD

This bit selects the AC frame drive waveform period. MOD is typically set to 1.
When this bit = 0, 16-line AC drive is selected.
When this bit = 1, two-frame AC drive is selected.

In two-frame AC drive, the MOD period is twice the frame period. In 16-line AC drive, MOD inverts every 16 lines. Although 16-line AC drive gives a more readable display, horizontal lines may appear when using high LCD drive voltages or at high viewing angles.

bits 3-0 Horizontal Character Size (FX) bits [3:0]

These bits define the horizontal size, or width, of each character, in pixels.

REG[01h] bits 3-0 = Horizontal Character Size in pixels - 1

The S1D13700F01 handles display data in 8-bit units, therefore characters larger than 8 pixels wide must be formed from 8-pixel segments. The following diagram shows an example of a character requiring two 8-pixel segments where the remainder of the second eight bits are not displayed. This also applies to the second screen layer. In graphics mode, the normal character field is also eight pixels. If a wider character field is used, any remainder in the second eight bits is not displayed.

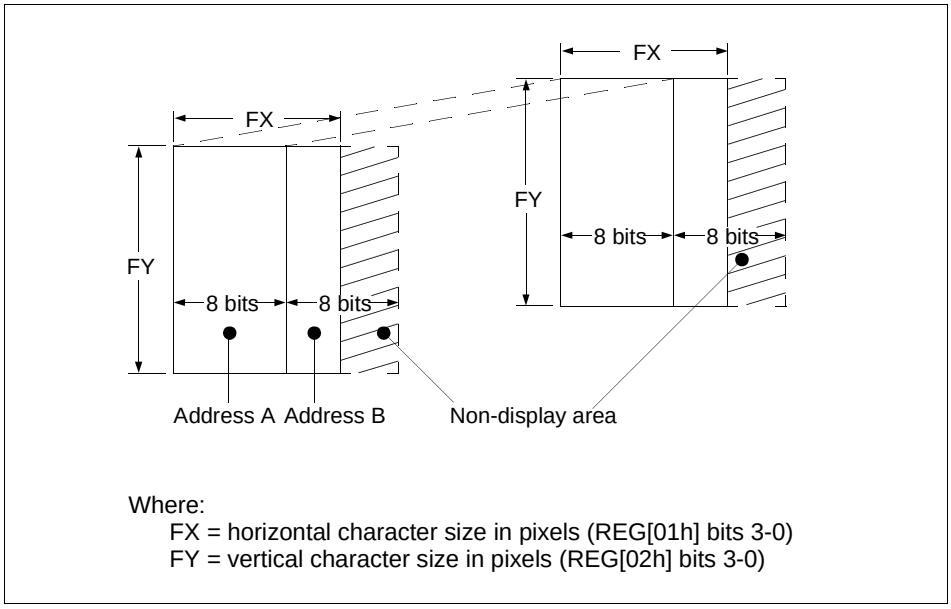


Figure 10-4 Horizontal and Vertical Character Size Example

REG[02h] Vertical Character Size Register
Address = 8002h Default = 00h Read/Write

7	6	5	4	3	2	1	0
n/a				Vertical Character Size bits 3-0			

bit 3-0 Vertical Character Size (FY) bits [3:0]
These bits define the vertical size, or height, of each character, in pixels.
REG[02h] bits 3-0 = Vertical Character Size in pixels - 1

REG[03h] Character Bytes Per Row Register
Address = 8003h Default = 00h Read/Write

7	6	5	4	3	2	1	0
Character Bytes Per Row bits 7-0							

bits 7-0 Character Bytes Per Row (C/R) bits [7:0]
These bits determine the size of each character row (or display line), in bytes, to a maximum of 239. The value of these bits is defined in terms of C/R which is calculated in Section 15.1.1, “SYSTEM SET Command and Parameters” on page 101.
REG[03h] bits 7-0 = ([C/R] x bpp) - 1

REG[04h] Total Character Bytes Per Row Register
Address = 8004h Default = 00h Read/Write

7	6	5	4	3	2	1	0
Total Character Bytes Per Row bits 7-0							

bits 7-0 Total Character Bytes Per Row (TC/R) bits [7:0]
These bits set the length of one line, including horizontal blanking, in bytes, to a maximum of 255. The value of these bits is defined in terms of TC/R which is calculated in Section 15.1.1, “SYSTEM SET Command and Parameters” on page 101. TC/R can be adjusted to hold the frame period constant and minimize jitter for any given main oscillator frequency, fosc.
REG[04h] bits 7-0 = [TC/R] + 1

Note
TC/R must be programmed such that the following formulas are valid.
$[TC/R] \geq [C/R] + 2$
$0 \leq [TC/R] \leq 255$

REG[05h] Frame Height Register
Address = 8005h Default = 00h Read/Write

Frame Height bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Frame Height (L/F) bits [7:0]
These bits determine the frame height, in lines. The maximum frame height is 256 lines.
REG[05h] bits 7-0 = frame height in lines - 1.

Note
If the Panel Drive Select bit is set for a dual drive panel (REG[00h] bit 3 = 1), the frame height must be an even number of lines resulting in an odd number value for REG[05h] bits 7-0.

REG[06h] Horizontal Address Range Register 0
Address = 8006h Default = 00h Read/Write

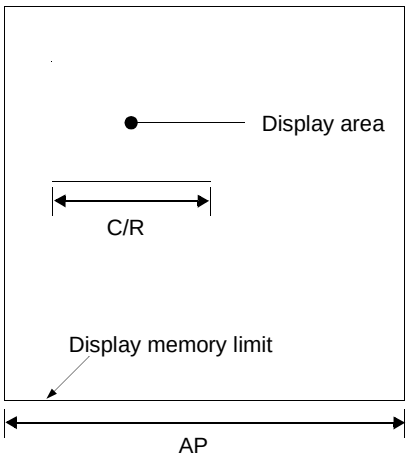
Horizontal Address Range bits 7-0							
7	6	5	4	3	2	1	0

REG[07h] Horizontal Address Range Register 1
Address = 8007h Default = 00h Read/Write

Horizontal Address Range bits 15-8							
7	6	5	4	3	2	1	0

bits 15-0 Horizontal Address Range (AP) bits [15:0]
These bits define the horizontal address range of the virtual screen. The maximum value for this register is 7FFFh.
REG[07h] bits 7-0, REG[06h] bits 7-0 = Addresses per line

The following diagram demonstrates the relationship between the Horizontal Address Range and the Character Bytes Per Row value.



Where:
C/R = character bytes per row (REG[03h] bits 7-0)
AP = horizontal address range (REG[06h] bits 7-0, REG[07h] bits 7-0)

Figure 10-5 Horizontal Address Range and Character Bytes Per Row Relationship

POWER SAVE

The POWER SAVE command is used to enter power save mode on the S1D13700F01 when indirect addressing is used. For further information on the POWER SAVE command, see Section 11.1.2, “POWER SAVE” on page 72.

Note

When indirect addressing is used, the SYSTEM SET command is used to exit power save mode. For further information on the SYSTEM SET command, see Section 11.1.1, “SYSTEM SET” on page 71.'

REG[08h] Power Save Mode Register

Address = 8008h Default = 01h Read/Write

7	6	5	4	3	2	1	0
n/a							Power Save Mode Enable

bit 0 Power Save Mode Enable

This bit controls the state of the software initiated power save mode. When power save mode is disabled, the S1D13700F01 is operating normally. When power save mode is enabled, the S1D13700F01 is in a power efficient state where all internal operations, including the oscillator, are stopped. For more information on the condition of the S1D13700F01 during Power Save Mode, see Section 17, “Power Save Mode” on page 125.

When this bit = 0, power save mode is disabled (see note).

When this bit = 1, power save mode is enabled (default).

Note

To fully disable power save mode when in Direct mode, a dummy write to any register must be performed after setting REG[08h] bit 0 = 0.

Note

Enabling power save mode automatically clears the Display Enable bit (REG[09h] bit 0). After power save mode is disabled, the Display Enable bit must be set (REG[09h] bit 0 = 1) in order to turn on the display again.

10.3.2 Display Control Registers

These registers enable/disable the display, and control the cursor and layered screens.

DISP ON/OFF

The DISP ON/OFF command is used to enable/disable the display and display attributes when indirect addressing is used. The values from REG[0Ah] are passed as parameters when the DISP ON/OFF command is issued. For further information on the DISP ON/OFF command, see Section 11.1.3, “DISP ON/OFF” on page 72.

REG[09h] Display Enable Register
Address = 8009h Default = 00h Read/Write

7	6	5	4	3	2	1	0
n/a							Display Enable

bit 0 Display Enable
This bit controls the LCD display, including the cursor and all layered screens. The display enable bit takes precedence over the individual attribute bits in the Display Attribute register, REG[0Ah]. For information on LCD pin states when the display is off (REG[09h] bit 0 = 0), see Table 17-1 “State of LCD Pins During Power Save Mode,” on page 125.
When this bit = 0, the display is off.
When this bit = 1, the display is on.

REG[0Ah] Display Attribute Register
Address = 800Ah Default = 00h Read/Write

7	6	5	4	3	2	1	0
SAD3 Attribute bits 1-0		SAD2 Attribute bits 1-0		SAD1 Attribute bits 1-0		Cursor Attribute bits 1-0	

bits 7-6 SAD3 Attribute (FP 5-4) bits [1:0]
These bits control the attributes of the third screen block (SAD3) as follows.

Table 10-3 Screen Block 3 Attribute Selection

Third Screen Block (SAD3)			
REG[0Ah] bit 7	**REG[0Ah] bit 6**	**Attributes**	
0	0	OFF (Blank)	
0	1	ON	No Flashing
1	0		Flash at f_{FR}/32 Hz (approx. 2 Hz)
1	1		Flash at f_{FR}/4 Hz (approx. 16 Hz)

bits 5-4 SAD2 Attribute (FP 3-2) bits [1:0]

These bits control the attributes of the second screen block (SAD2). These bits also control the attributes of the fourth screen block (SAD4) when it is enabled by setting the Panel Drive Select bit to dual panel mode (REG[00h] bit 3 = 1). In this mode, the attributes of the second screen block (SAD2) and the fourth screen block (SAD4) share the same settings and cannot be set independently.

Table 10-4 Screen Block 2/4 Attribute Selection

Second Screen Block (SAD2, SAD4)			
REG[0Ah] bit 5	**REG[0Ah] bit 4**	**Attributes**	
0	0	OFF (Blank)	
0	1	ON	No Flashing
1	0		Flash at f_{FR}/32 Hz (approx. 2 Hz)
1	1		Flash at f_{FR}/4 Hz (approx. 16 Hz)

bits 3-2 SAD1 Attribute (FP 1-0) bits [1:0]

These bits control the attributes of the first screen block (SAD1) as follows.

Table 10-5 Screen Block Attribute Selection

First Screen Block (SAD1)			
REG[0Ah] bit 3	**REG[0Ah] bit 2**	**Attributes**	
0	0	OFF (Blank)	
0	1	ON	No Flashing
1	0		Flash at f_{FR}/32 Hz (approx. 2 Hz)
1	1		Flash at f_{FR}/4 Hz (approx. 16 Hz)

bits 1-0 Cursor Attribute (FC) bits [1:0]

These bits control the cursor and set the flash rate. The cursor flashes with a 70% duty cycle (ON 70% of the time and OFF 30% of the time).

Table 10-6 Cursor Flash Rate Selection

Bit 1	Bit 0	Cursor Display	
0	0	OFF (Blank)	
0	1	ON	No Flashing
1	0	ON	Flash at f_{FR}/32 Hz (approx. 2 Hz)
1	1	ON	Flash at f_{FR}/64 Hz (approx. 1 Hz)

Note

When the cursor is disabled, a write to memory automatically enables the cursor and places the cursor at the next memory location. A read from memory does not enable the cursor, however, it still places the cursor at the next memory location.

SCROLL

The SCROLL command is used to configure the display start addresses for the various screen blocks when indirect addressing is used. The values from REG[0Bh] through REG[14h] are passed as parameters when the SCROLL command is issued. For further information on the SCROLL command, see Section 11.1.4, “SCROLL” on page 73.

REG[0Bh] Screen Block 1 Start Address Register 0
Address = 800Bh Default = 00h Read/Write

Screen Block 1 Start Address bits 7-0 (LSB)							
7	6	5	4	3	2	1	0

REG[0Ch] Screen Block 1 Start Address Register 1
Address = 800Ch Default = 00h Read/Write

Screen Block 1 Start Address bits 15-8 (MSB)							
7	6	5	4	3	2	1	0

bits 15-0 Screen Block 1 Start Address (SAD1) bits [15:0]
These bits determine the memory start address of screen block 1.

Note
When the start address is changed, the LSB must be programmed before the MSB. The start address does not change until the MSB is written.

REG[0Dh] Screen Block 1 Size Register
Address = 800Dh Default = 00h Read/Write

Screen Block 1 Size bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Screen Block 1 Size (SL1) bits [7:0]
These bits determine the size of screen block 1, in lines.
REG[0Dh] bits 7-0 = screen block 1 size in number of lines - 1

Note
The relationship between the screen block start address (SADx), screen block size (SLx), and the display mode is described in Table 10-7 “Display Modes,” on page 58.

REG[0Eh] Screen Block 2 Start Address Register 0

Address = 800Eh Default = 00h Read/Write

Screen Block 2 Start Address bits 7-0 (LSB)							
7	6	5	4	3	2	1	0

REG[0Fh] Screen Block 2 Start Address Register 1

Address = 800Fh Default = 00h Read/Write

Screen Block 2 Start Address bits 15-8 (MSB)							
7	6	5	4	3	2	1	0

bits 15-0 Screen Block 2 Start Address (SAD2) bits [15:0]

These bits determine the memory start address of screen block 2.

Note

When the start address is changed, the LSB must be programmed before the MSB. The start address does not change until the MSB is written.

REG[10h] Screen Block 2 Size Register

Address = 8010h Default = 00h Read/Write

Screen Block 2 Size bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Screen Block 2 Size (SL2) bits [7:0]

These bits determine the size of screen block 2, in lines.

REG[10h] bits 7-0 = screen block 2 size in number of lines - 1

Note

The relationship between the screen block start address (SADx), screen block size (SLx), and the display mode is described in Table 10-7 “Display Modes,” on page 58.

REG[11h] Screen Block 3 Start Address Register 0
Address = 8011h Default = 00h Read/Write

Screen Block 3 Start Address bits 7-0 (LSB)							
7	6	5	4	3	2	1	0

REG[12h] Screen Block 3 Start Address Register 1
Address = 8012h Default = 00h Read/Write

Screen Block 3 Start Address bits 15-8 (MSB)							
7	6	5	4	3	2	1	0

bits 15-0 Screen Block 3 Start Address (SAD3) bits [15:0]
These bits determine the memory start address of screen block 3.

Note
When the start address is changed, the LSB must be programmed before the MSB. The start address does not change until the MSB is written.

REG[13h] Screen Block 4 Start Address Register 0
Address = 8013h Default = 00h Read/Write

Screen Block 4 Start Address bits 7-0 (LSB)							
7	6	5	4	3	2	1	0

REG[14h] Screen Block 4 Start Address Register 1
Address = 8014h Default = 00h Read/Write

Screen Block 4 Start Address bits 15-8 (MSB)							
7	6	5	4	3	2	1	0

bits 15-0 Screen Block 4 Start Address (SAD4) bits [15:0]
These bits determine the memory start address of screen block 4.

Note
When the start address is changed, the LSB must be programmed before the MSB. The start address does not change until the MSB is written.

The following table summaries the required settings for each possible display mode.

Table 10-7 Display Modes

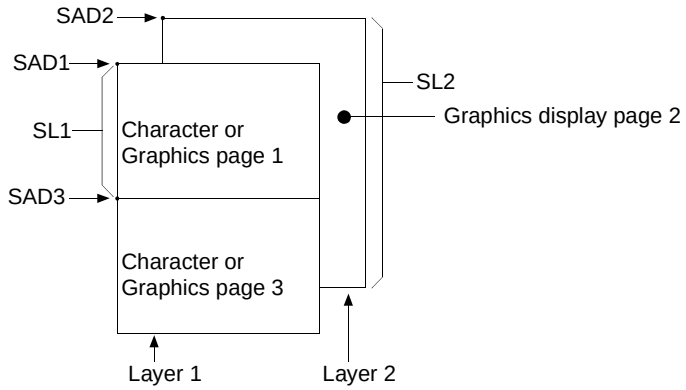
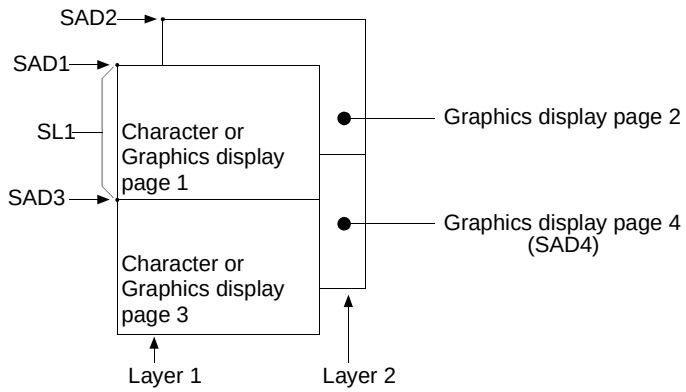
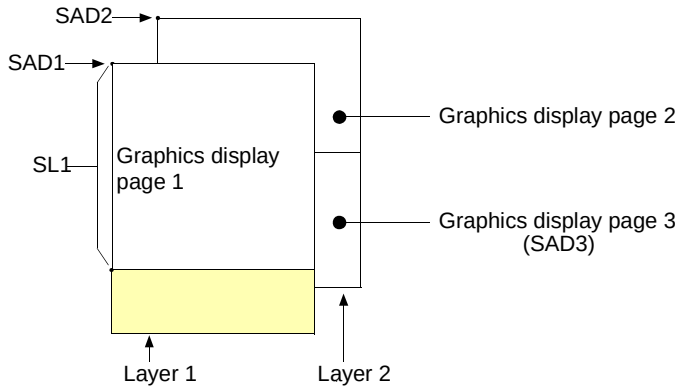
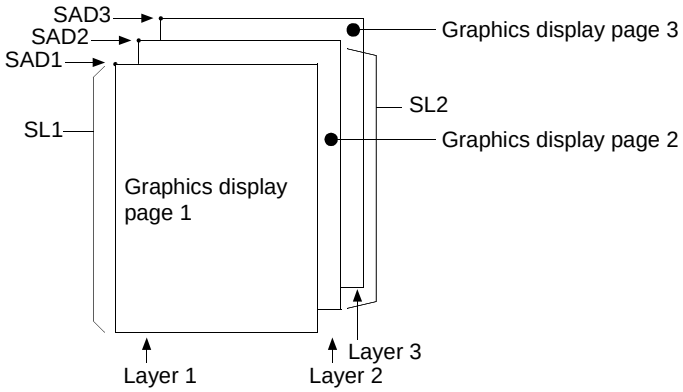
<table>
<tr><th>REG[00h] bit 3 (W/S)</th><th>Screen</th><th>First Layer</th><th>Second Layer</th></tr>
<tr><td rowspan="4">0</td><td>First Screen Block</td><td>SAD1</td><td>SAD2</td></tr>
<tr><td>Second Screen Block</td><td>SL1</td><td>SL2</td></tr>
<tr><td>Third Screen Block (partitioned screen)</td><td colspan="2">SAD3 (see note 1)
Set both SL1 and SL2 to L/F + 1 if not using a partitioned screen.</td></tr>
<tr><td colspan="3">Screen Configuration Example

</td></tr>
<tr><td rowspan="4">1</td><td>First Screen Block</td><td>SAD1, SL1</td><td>SAD2, SL2</td></tr>
<tr><td>Second Screen Block</td><td>SAD3 (see note 2)</td><td>SAD4 (see note 2)</td></tr>
<tr><td colspan="3">Set both SL1 and SL2 to ([L/F] ÷ 2 + 1)</td></tr>
<tr><td colspan="3">Screen Configuration Example

</td></tr>
</table>

Table 10-7 Display Modes (Continued)

REG[00h] bit 3 (W/S)	Screen	First Layer	Second Layer	
0	First Screen Block	SAD1, SL1	SAD2, SL2	
	Second Screen Block	—	SAD3 (see note 2)	
	Set SL1 > SL2			
	Screen Configuration Example  			
REG[00h] bit 3 (W/S)	**Screen**	**First Layer**	**Second Layer**	**Third Layer**
0	Three-Layer Configuration	SAD1, SL1 = L/F + 1	SAD2, SL2 = L/F + 1	SAD3
	Screen Configuration Example  			

Note

1 The size of screen block 3, in lines, is automatically set to the size of the screen block with the least number of lines (either SL1 or SL2).

2 The parameters corresponding to SL3 and SL4 are fixed by REG[05h] bits 7-0 (L/F) and do not have to be set.

3 If a dual panel is selected (REG[00h] bit 3 = 1), the differences between SL1 and (L/F + 1) ÷ 2, and between SL2 and (L/F + 1) ÷ 2, are blanked.

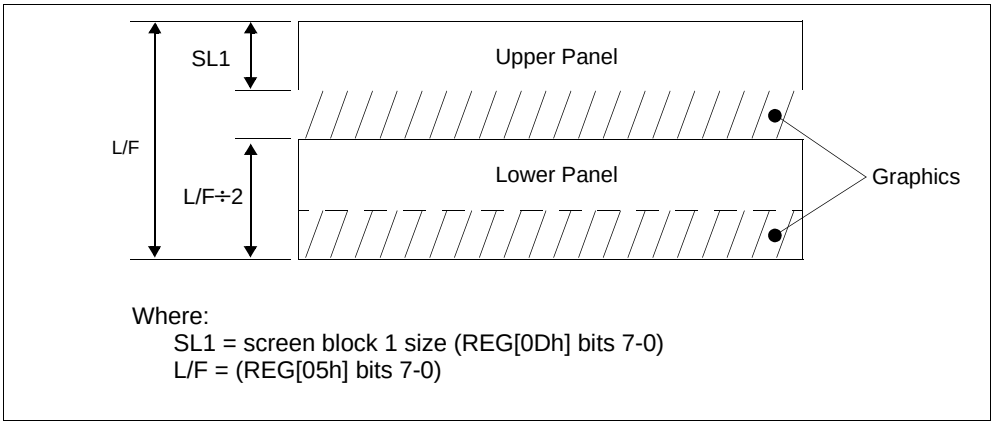


Figure 10-6 Dual Panel Display Height

CSRFORM

The CSRFORM command is used to configure the S1D13700F01 cursor when indirect addressing is used. The values from REG[15h] through REG[16h] are passed as parameters when the CSRFORM command is issued. For further information on the CSRFORM command, see Section 11.1.5, “CSRFORM” on page 73.

The cursor registers are used to set the size, shape, and position of the cursor. Although the cursor is normally only used for text displays, it may be used for graphics displays when displaying special characters.

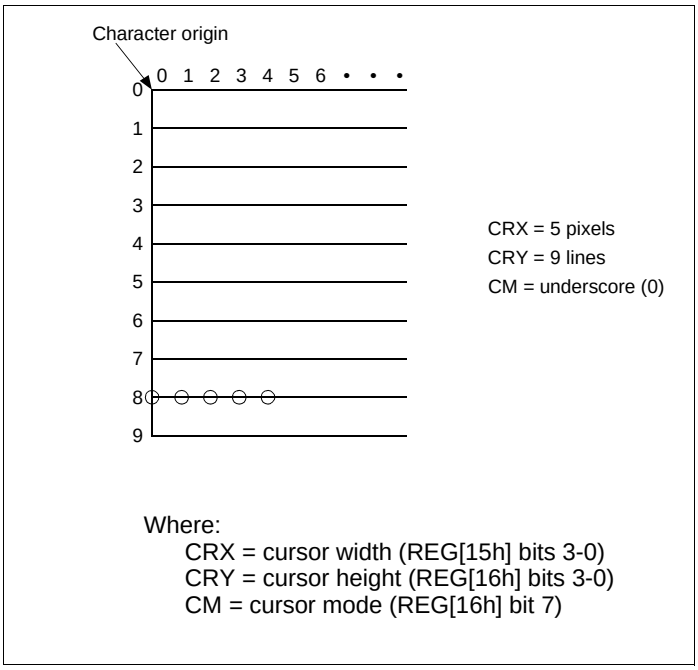


Figure 10-7 Cursor Size and Position

REG[15h] Cursor Width Register
Address = 8015h Default = 00h Read/Write

n/a				Cursor Width bits 3-0			
7	6	5	4	3	2	1	0

bits 3-0 Cursor Width (CRX) bits[3:0]
These bits specify the width (or horizontal size) of the cursor, in pixels from the character origin (see Figure 10-7 “Cursor Size and Position,” on page 60).
REG[15h] bits 3-0 = cursor width in pixels - 1

Note
The cursor width must be less than or equal to the horizontal character size.
(REG[16h] bits 3-0 <= REG[01h] bits 3-0)

REG[16h] Cursor Height Register
Address = 8016h Default = 00h Read/Write

Cursor Mode	n/a			Cursor Height bits 3-0			
7	6	5	4	3	2	1	0

bit 7 Cursor Mode (CM)
This bit determines the cursor mode. When graphics mode is selected, this bit must be set to 1.
When this bit = 0, an underscore cursor (_) is selected.
When this bit = 1, a block cursor (■) is selected.

bits 3-0 Cursor Height (CRY) bits [3:0]
For an underscore cursor (REG[16h] bit 7 = 0), these bits set the location of the cursor, in lines from the character origin (see Figure 10-7 “Cursor Size and Position,” on page 60).
For a block cursor (REG[16h] bit 7 = 1), these bits set the height (or vertical size) of the cursor, in lines from the character origin (see Figure 10-7 “Cursor Size and Position,” on page 60).
REG[16h] bits 3-0 = cursor height in lines - 1

Note
The vertical cursor size must be less than or equal to the vertical character size.
(REG[16h] bits 3-0 <= REG[02h] bits 3-0)

CSRDIR

The CSRDIR command controls cursor movement when indirect addressing is used. The values from REG[17h] are passed as part of the command when the CSRDIR command is issued. For further information on the CSRDIR command, see Section 11.1.6, “CSRDIR” on page 74.

REG[17h] Cursor Shift Direction Register
Address = 8017h Default = 00h Read/Write

n/a						Cursor Shift Direction bits 1-0	
7	6	5	4	3	2	1	0

bits 1-0 Cursor Shift Direction bits [1:0]

These bits set the direction of automatic cursor increment when the cursor is automatically moved after a memory access (read or write). The cursor can move left/right by one character or up/down by the number of bytes specified by the horizontal address range (or address pitch), REG[06h] - REG[07h]. When reading from and writing to display memory, this automatic cursor increment controls the display memory address increment on each read or write.

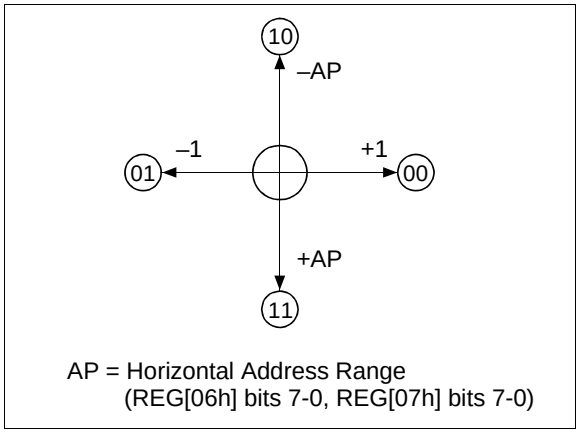


Figure 10-8 Cursor Direction

Table 10-8 Cursor Shift Direction

Direct Mode		Indirect Mode Command	Shift Direction
Bit 1	Bit 0		
0	0	4C	Right
0	1	4D	Left
1	0	4E	Up
1	1	4F	Down

Note

The cursor moves in address units even if horizontal character size is equal to 9 (REG[01h] bits 3-0 = 9), therefore the cursor address increment must be preset for movement in character units. For further information, see Section 12.3, “Cursor Control” on page 84.

OVLAY

The OVLAY command selects layered screen composition and screen text/graphics mode when indirect addressing is used. The values from REG[18h] are passed as parameters when the OVLAY command is issued. For further information on the OVLAY command, see Section 11.1.7, “OVLAY” on page 74.

REG[18h] Overlay Register
Address = 8018h Default = 00h Read/Write

n/a			3 Layer Overlay Select	Screen Block 3 Display Mode	Screen Block 1 Display Mode	Layer Composition Method bits 1-0	
7	6	5	4	3	2	1	0

bit 4 3 Layer Overlay Select (OV)
This bit determines how many layers are used when graphics mode is enabled. For mixed text and graphics, this bit must be set to 0.
When this bit = 0, two layers are used.
When this bit = 1, three layers are used.

bit 3 Screen Block 3 Display Mode (DM1)
This bit determines the display mode for screen block 3.
When this bit = 0, screen block 3 is configured for text mode.
When this bit = 1, screen block 3 is configured for graphics mode.

Note
Screen blocks 2 and 4 can display graphics only.

bit 2 Screen Block 1 Display Mode (DM0)
This bit determines the display mode for screen block 1.
When this bit = 0, screen block 1 is configured for text mode.
When this bit = 1, screen block 1 is configured for graphics mode.

Note
Screen blocks 2 and 4 can display graphics only.

bits 1-0 Layer Composition Method (MX) bits [1:0]
These bits select the layered screen composition method, which can be OR, AND, or Exclusive-OR. Since the screen composition is organized in layers and not by screen blocks, when using a layer divided into two screen blocks, different composition methods cannot be specified for the individual screen blocks.

Table 10-9 Composition Method Selection

REG[18h] bit 1	REG[18h] bit 0	Function	Composition Method	Applications
0	0	L1 ∪ L2 ∪ L3	OR	Underlining, rules, mixed text and graphics
0	1	(L1 ⊕ L2) ∪ L3	Exclusive-OR	Inverted characters, flashing regions, underlining
1	0	(L1 ∩ L2) ∪ L3	AND	Simple animation, three-dimensional appearance
1	1	—	—	Reserved

Note
L1: First layer (text or graphics). If text is selected, layer L3 cannot be used.
L2: Second layer (graphics only)
L3: Third layer (graphics only)

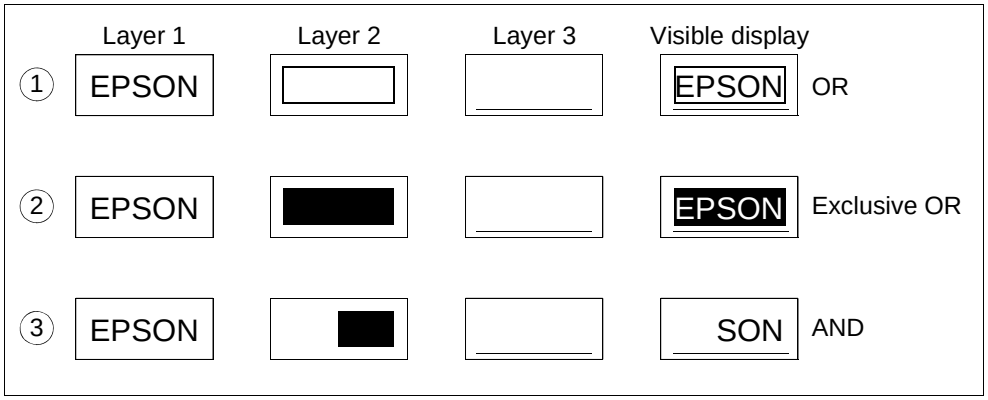


Figure 10-9 Combined Layer Display Examples

Note
L1: Not flashing
L2: Flashing at 1 Hz
L3: Flashing at 2 Hz

CGRAM ADR

The CGRAM ADR command sets the start address of the character generator RAM (CGRAM) when indirect addressing is used. The values from REG[19h] through REG[1Ah] are passed as parameters when the CGRAM ADR command is issued. For further information on the CGRAM ADR command, see Section 11.1.8, “CGRAM ADR” on page 74.

REG[19h] Character Generator RAM Start Address Register 0
Address = 8019h Default = 00h Read/Write

7	6	5	4	3	2	1	0
CGRAM Start Address bits 7-0 (LSB)							

REG[1Ah] Character Generator RAM Start Address Register 1
Address = 801Ah Default = 00h Read/Write

7	6	5	4	3	2	1	0
CGRAM Start Address bits 15-8 (MSB)							

bits 15-0 Character Generator RAM Start Address bits [15:0]
These bits determine the memory start address of the Character Generator RAM (CGRAM). The exact memory location of the start of each character stored in CGRAM can be calculated by multiplying the character code index by the character height and adding the total to the CGRAM start address.

For example, to determine the address of a 8x8 character at character code index 80h with a CGRAM start address of 6000h, the following calculation can be used.

character start = (character code index x character height) + CGRAM start address
= (80h x 8) + 6000h
= 400h + 6000h
= 6400h

The character starts in RAM at address 6400h and takes 8 memory locations.

HDOT SCR

The HDOT SCR command sets the horizontal scroll position when indirect addressing is used. The values from REG[1Bh] are passed as parameters when the HDOT SCR command is issued. For further information on the HDOT SCR command, see Section 11.1.9, "HDOT SCR" on page 75.

Normal scrolling on text screens allows scrolling of entire characters only. The HDOT SCR command provides horizontal pixel scrolling for text screens. HDOT SCR cannot be used on individual layers.

Note
HDOT SCR must be set to zero for all display modes except 1 bpp (REG[20h] Bit-Per-Pixel Select Register bits 1-0 = 0).

REG[1Bh] Horizontal Pixel Scroll Register
Address = 801Bh Default = 00h Read/Write

n/a					Horizontal Pixel Scroll bits 2-0		
7	6	5	4	3	2	1	0

bits 2-0 Horizontal Pixel Scroll bits [2:0]
These bits specify the number of horizontal pixels to scroll the display. The character bytes per row (C/R), REG[03h] bits 7-0, must be set to one more than the actual number of horizontal characters before using horizontal pixel scroll. Smooth scrolling can be simulated by repeatedly changing the value of REG[1Bh] bits 2-0. See Section 12.5, "Scrolling" on page 90 for more information on scrolling the display.

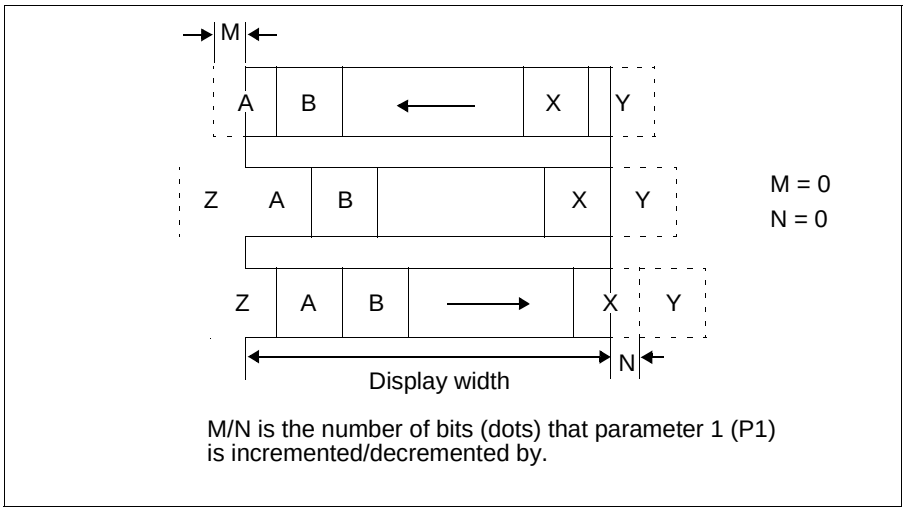


Figure 10-10 Horizontal Scrolling

10.3.3 Drawing Control Registers

CSRW

The CSRW command sets the cursor address when indirect addressing is used. The values from REG[1Ch] through REG[1Dh] are passed as parameters when the CSRW command is issued. For further information on the CSRW command, see Section 11.1.10, “CSRW” on page 75.

REG[1Ch] Cursor Write Register 0
Address = 801Ch Default = 00h Write Only

Cursor Write bits 7-0 (LSB)							
7	6	5	4	3	2	1	0

REG[1Dh] Cursor Write Register 1
Address = 801Dh Default = 00h Write Only

Cursor Write bits 15-8 (MSB)							
7	6	5	4	3	2	1	0

bits 15-0 Cursor Write (CSRW) bits [15:0]
These bits set the display memory address to the data at the cursor position as shown in Figure 12-10 “Cursor Movement,” on page 86.

Note
The microprocessor cannot directly access the display memory in indirect addressing mode.

For Indirect Addressing Mode:

The MREAD and MWRITE commands use the address in this register when in indirect mode. The cursor address register can only be modified by the CSRW command, and by the automatic increment after an MREAD or MWRITE command. It is not affected by display scrolling.

If a new address is not set, display memory accesses are from the last set address or the address after previous automatic increments.

CSRR

The CSRR command reads the cursor address when indirect addressing is used. The values from REG[1Eh] through REG[1Fh] are passed as parameters when the CSRR command is issued. For further information on the CSRR command, see Section 11.1.11, “CSRR” on page 75.

REG[1Eh] Cursor Read Register 0
Address = 801Eh Default = 00h Read Only

Cursor Read bits 7-0 (LSB)							
7	6	5	4	3	2	1	0

REG[1Fh] Cursor Read Register 1
Address = 801Fh Default = 00h Read Only

Cursor Read bits 15-8 (MSB)							
7	6	5	4	3	2	1	0

bits 15-0 Cursor Read (CSRR) bits [15:0]

These bits are only used in Indirect Addressing mode.

These bits indicate the memory address where the cursor is currently located. After issuing the command, the data read address is read twice. Once for the low byte and then again for the high byte of the register.

10.3.4 Gray Scale Register

GRAYSCALE

The GRAYSCALE command selects the gray scale depth, in bits-per-pixel (bpp), when indirect addressing is used. The values from REG[20h] are passed as parameters when the GRAYSCALE command is issued. For further information on the GRAYSCALE command, see Section 11.1.12, “GRAYSCALE” on page 76.

Note
When a graphics screen and a graphics screen with Gray Scale enabled are overlaid, both layers must be configured for the same color depth. For example, if the first layer is 2 bpp, the second layer must also be set for 2 bpp.

REG[20h] Bit-Per-Pixel Select Register
Address = 8020h Default = 00h Read/Write

n/a						Bit-Per-Pixel Select bits 1-0	
7	6	5	4	3	2	1	0

bits 1-0 Bit-Per-Pixel Select bits [1:0]
These bits select the bit-per-pixel mode as follows. If the CGRAM is used (includes CGRAM1 and CGRAM2), only 1 bpp is supported.

Table 10-10 Bit-Per-Pixel Selection

REG[20h] bits 1-0	Bits-Per-Pixel
00	1
01	2
10	4
11	Reserved

Note
The horizontal character size (REG[01h] bits 3-0) must be set to 7h and the Horizontal Pixel Scroll bits (REG[1Bh] bits 2-0) must be set to 0.

11 Indirect Addressing

Table 11-1 Indirect Addressing Command Set

Class	Register Address	Command	Register Description	Control Byte Value	No. of Bytes
System Control	8000h - 8007h	SYSTEM SET	Initializes device and display	40h	8
	8008h	POWER SAVE	Enters standby mode	53h	0
Display Control	8009h - 800A	DISP ON/OFF	Enables/disables display and display attributes	58h 59h	1
	800Bh - 8014h	SCROLL	Sets screen block start addresses and sizes	44h	10
	8015h - 8016h	CSRFORM	Sets cursor type	5Dh	2
	8017h	CSRDIR	Sets direction of cursor movement	4Ch - 4Fh	0
	8018h	OVLAY	Sets display overlay format	5Bh	1
	8019h - 801Ah	CGRAM ADR	Sets start address of character generator RAM	5Ch	2
	801Bh	HDOT SCR	Sets horizontal scroll position	5A	1
Drawing Control	801Ch - 801Dh	CSRW	Sets cursor address	46h	2
	801Eh - 801Fh	CSRR	Reads cursor address	47h	2
	8020h	GRAYSCALE	Sets the Grayscale depth (bpp)	60h	1
Memory Control		MEMWRITE	Writes to memory	42h	n/a
		MEMREAD	Reads from memory	43h	

Table 11-2 Generic Indirect Addressing Command/Write/Read

A0	$\overline{WR}$	$\overline{RD}$	
1	0	1	Command [C]
1	1	0	Parameter Read [P#]
0	0	1	Parameter Write [P#]

Table 11-3 M6800 Indirect Addressing Command/Write/Read

A0	R/$\overline{W}$	E	
1	0	1	Command write
1	1	1	Display data and cursor address read
0	0	1	Display data and parameter write

Table 11-4 M68K Indirect Addressing Command/Write/Read

A0	R/$\overline{W}$	LDS#	
1	0	0	Command write
1	1	0	Display data and cursor address read
0	0	0	Display data and parameter write

11.1 System Control

See Section 15.1.2, “Initialization Example” on page 104 for the initialization sequence.

11.1.1 SYSTEM SET

See Section , “SYSTEM SET” on page 45 for further information.

Note
If the S1D13700F01 is in power save mode (at power up or after a POWER SAVE command), the SYSTEM SET command will exit power save mode. After writing the SYSTEM SET command and its 8 parameters, the S1D13700F01 will be in normal operation.

Table 11-5 SYSTEM SET Command and Parameters

MSB							LSB	
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**	**Indirect**
0	1	0	0	0	0	0	0	C
0	0	IV[1]	0	W/S[2]	M2[3]	0	M0[4]	P1
MOD[5]	0	0	0	REG[01h] bits 3-0				P2
0	0	0	0	REG[02h] bits 3-0				P3
REG[03h] bits 7-0								P4
REG[04h] bits 7-0								P5
REG[05h] bits 7-0								P6
REG[06h] bits 7-0								P7
REG[07h] bits 7-0								P8

Note
[1] IV is the Screen Origin Compensation bit, REG[00h] bit 5.
[2] W/S is the Panel Drive Select bit, REG[00h] bit 3.
[3] M2 is the Character Height bit, REG[00h] bit 2.
[4] M0 is the Character Generator Select bit, REG[00h] bit 0.
[5] MOD is defined by REG[01h] bit 7.

11.1.2 POWER SAVE

See Section , “POWER SAVE” on page 52 for further information.

Table 11-6 POWER SAVE Command

MSB							LSB	
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**	**Indirect**
0	1	0	1	0	0	1	1	C

11.1.3 DISP ON/OFF

The following parameters are used for the DISP ON command. For further details, see Section , “DISP ON/OFF” on page 53.

Table 11-7 DISP ON Command and Parameters

MSB							LSB	
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**	**Indirect**
0	1	0	1	1	0	0	1	C
REG[0Ah] bits 7-0								P1

The following parameters are used for the DISP OFF command. For further details, see Section , “DISP ON/OFF” on page 53.

Table 11-8 DISP OFF Command and Parameters

MSB							LSB	
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**	**Indirect**
0	1	0	1	1	0	0	0	C
REG[0Ah] bits 7-0								P1

11.1.4 SCROLL

See "SCROLL" on page 55 for further information.

Table 11-9 SCROLL Command and Parameters

MSB bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	LSB bit 0		Indirect
0	1	0	0	0	1	0	0		C
A7	A6	A5	A4	A3	A2	A1	A0	REG[0Bh] bits 7-0	P1
A15	A14	A13	A12	A11	A10	A9	A8	REG[0Ch] bits 7-0	P2
L7	L6	L5	L4	L3	L2	L1	L0	REG[0Dh] bits 7-0	P3
A7	A6	A5	A4	A3	A2	A1	A0	REG[0Eh] bits 7-0	P4
A15	A14	A13	A12	A11	A10	A9	A8	REG[0Fh] bits 7-0	P5
L7	L6	L5	L4	L3	L2	L1	L0	REG[10h] bits 7-0	P6
A7	A6	A5	A4	A3	A2	A1	A0	REG[11h] bits 7-0	P7
A15	A14	A13	A12	A11	A10	A9	A8	REG[12h] bits 7-0	P8
A7	A6	A5	A4	A3	A2	A1	A0	REG[13h] bits 7-0	P9
A15	A14	A13	A12	A11	A10	A9	A8	REG[14h] bits 7-0	P10

Note
Set parameters P9 and P10 only if both dual panel (REG[00h] bit 3 = 1) and two-layer configuration are selected. SAD4 is the fourth screen block display start address.

11.1.5 CSRFORM

See "CSRFORM" on page 60 for further information.

Table 11-10 CSRFORM Command and Parameters

MSB bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	LSB bit 0	Indirect
0	1	0	1	1	1	0	1	C
0	0	0	0	REG[15h] bits 3-0 X3	X2	X1	X0	P1
CM[1]	0	0	0	REG[16h] bits 3-0 Y3	Y2	Y1	Y0	P2

Note
[1] CM is the Cursor Mode bit, REG[16h] bit 7.

11.1.6 CSRDIR

See "CSRDIR" on page 62 for further information.

Table 11-11 CSRDIR Command

MSB							LSB	
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**	**Indirect**
0	1	0	0	1	1	REG[17h] bits 1-0		
						CD1	CD0	C

11.1.7 OVLAY

See "OVLAY" on page 63 for further information.

Table 11-12 OVLAY Command and Parameters

MSB							LSB	
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**	**Indirect**
0	1	0	1	1	0	1	1	C
0	0	0	OV[1]	DM2[2]	DM1[2]	MX1[3]	MX0[3]	P1

Note
[1] OV is the 3 Layer Overlay Select bit, REG[18h] bit 4.
[2] DM2 and DM1 are the Screen Block 3/1 Display Mode bits, REG[18h] bits 3-2.
[3] MX1 and MX0 are the Layer Composition Method bits, REG[18h] bits 1-0.

11.1.8 CGRAM ADR

See "CGRAM ADR" on page 65 for further information.

Table 11-13 CGRAM ADR Command and Parameters

MSB							LSB		
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**		**Indirect**
0	1	0	1	1	1	0	0		C
A7	A6	A5	A4	A3	A2	A1	A0	(SAGL)	P1
A15	A14	A13	A12	A11	A10	A9	A8	(SAGH)	P2

11.1.9 HDOT SCR

See "HDOT SCR" on page 66 for further information.

Table 11-14 HDOT SCR Command and Parameters

MSB							LSB	
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**	**Indirect**
0	1	0	1	1	0	1	0	C
0	0	0	0	0	D2	D1	D0	P1

11.1.10 CSRW

See "CSRW" on page 67 for further information.

Table 11-15 CSRW Command and Parameters

MSB							LSB		
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**		**Indirect**
0	1	0	0	0	1	1	0		C
A7	A6	A5	A4	A3	A2	A1	A0	(CSRL)	P1
A15	A14	A13	A12	A11	A10	A9	A8	(CSRH)	P2

11.1.11 CSRR

See "CSRR" on page 68 for further information.

Table 11-16 CSRR Command and Parameters

MSB							LSB		
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**		**Indirect**
0	1	0	0	0	1	1	1		C
A7	A6	A5	A4	A3	A2	A1	A0	(CSRL)	P1
A15	A14	A13	A12	A11	A10	A9	A8	(CSRH)	P2

11.1.12 GRAYSCALE

See Section , “GRAYSCALE” on page 69 for further information.

Table 11-17 Gray Scale Command and Parameters

MSB							LSB	
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**	**Indirect**
0	1	1	0	0	0	0	0	C
0	0	0	0	0	0	BPP1	BPP0	P1

11.1.13 Memory Control

See “Drawing Control Registers” on page 67 for further information.

12 Display Control Functions

12.1 Character Configuration

The origin of each character bitmap is the top left corner as shown in Figure 12-1. Adjacent bits in each byte are horizontally adjacent in the corresponding character image.

Although the size of the bitmap is fixed by the character generator, the actual displayed size of the character field can be varied in both dimensions.

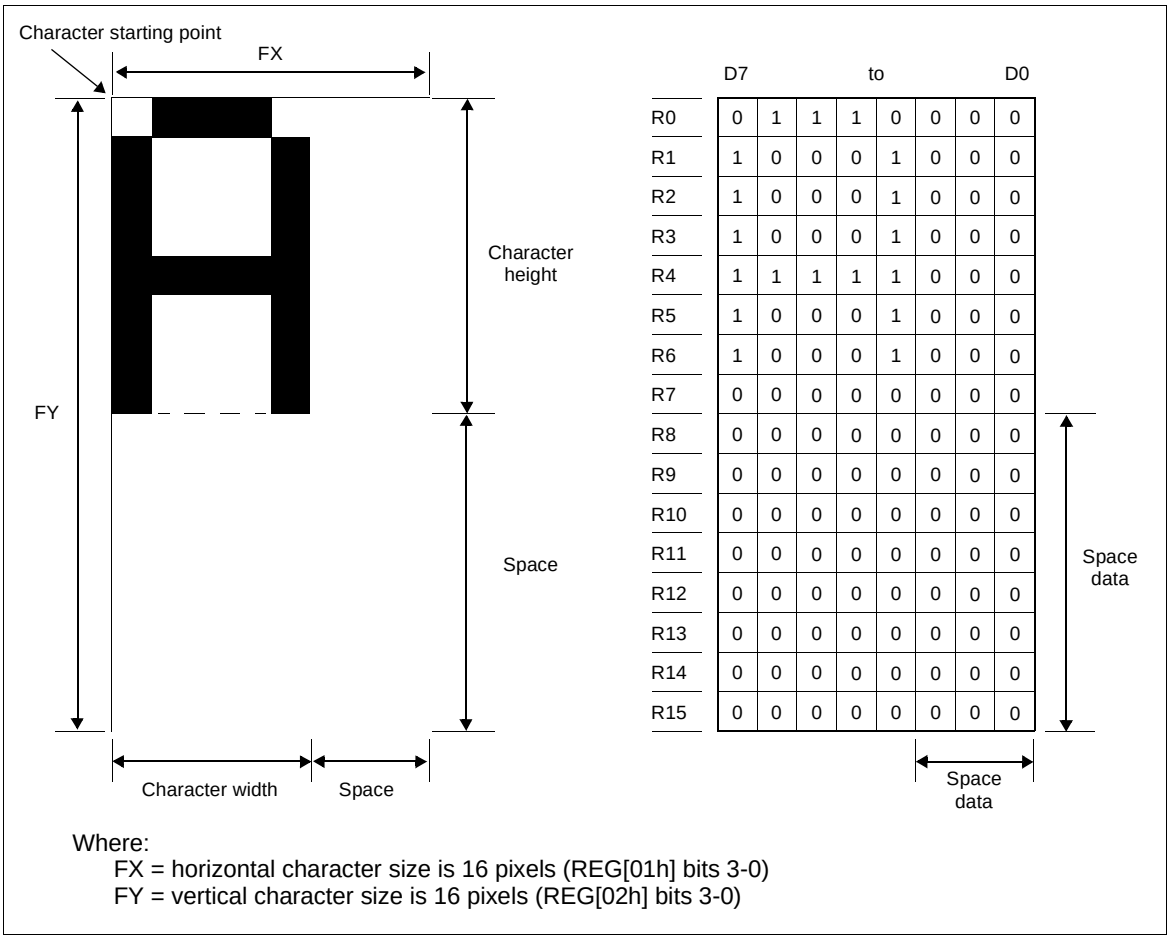


Figure 12-1 Example of Character Display from Generator Bitmap (when [FX] ≤ 8)

If the area outside the character bitmap contains only zeros, the displayed character size can be increased by increasing the horizontal character size (REG[01h] bits 3-0) and the vertical character size (REG[01h] bits 3-0). The zeros ensure that the extra space between displayed characters is blank.

The displayed character width can be set to any value up to 16 even if each horizontal row of the bitmap is two bytes wide.

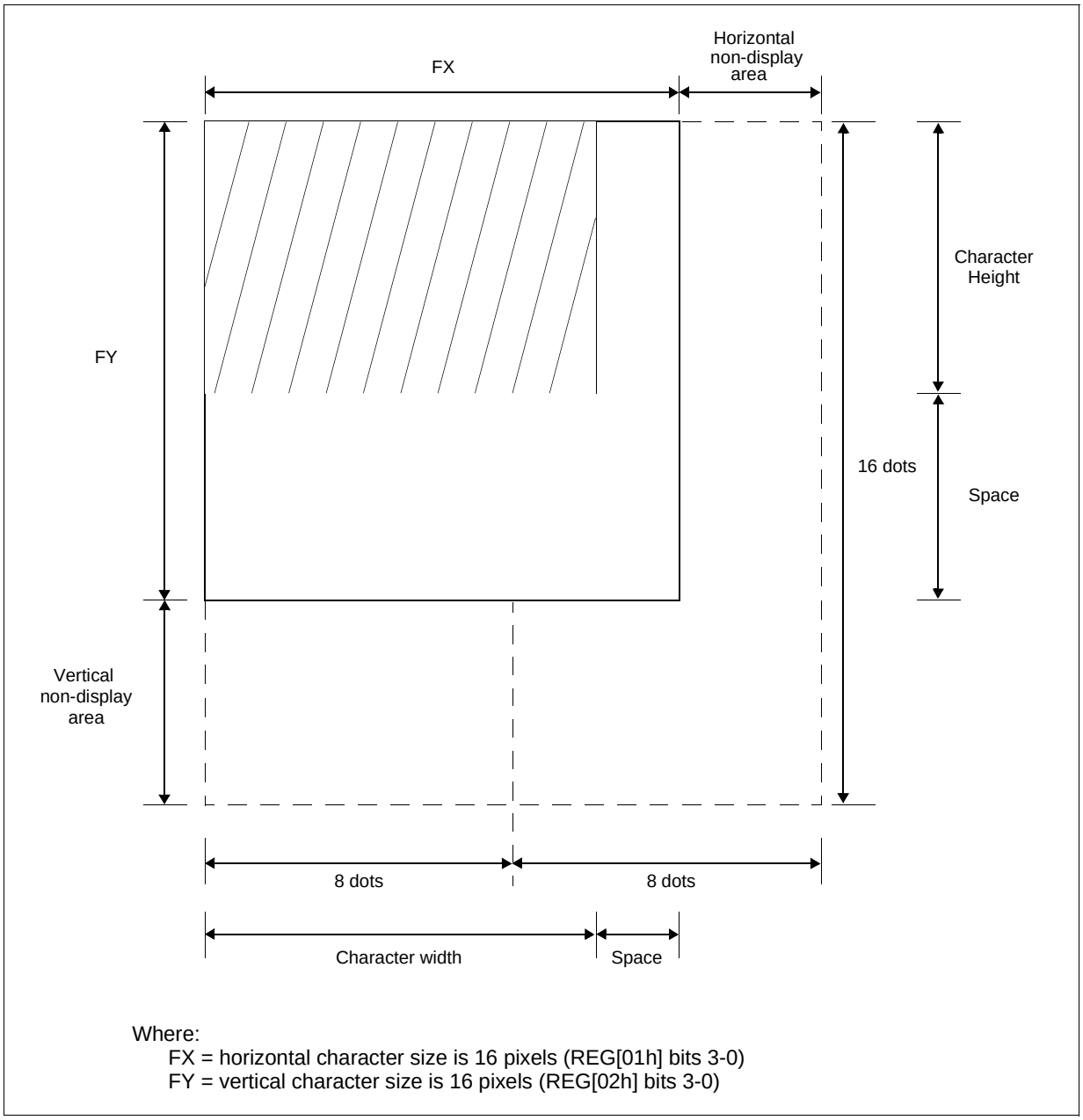


Figure 12-2 Character Width Greater than One Byte Wide ([FX] = 9)

Note

The S1D13700F01 does not automatically insert spaces between characters. If the displayed character size is 8 pixels or less and the space between character origins is nine pixels or more, the bitmap must use two bytes per row, even though the character image requires only one.

12.2 Screen Configuration

12.2.1 Screen Configuration

The S1D13700F01 can be configured for a single text screen, overlapping text screens, or overlapping graphics screens. Graphics screens use eight times as much display memory as a text screen in 1 bpp. Figure 12-3 shows the relationship between the virtual screens and the physical screen.

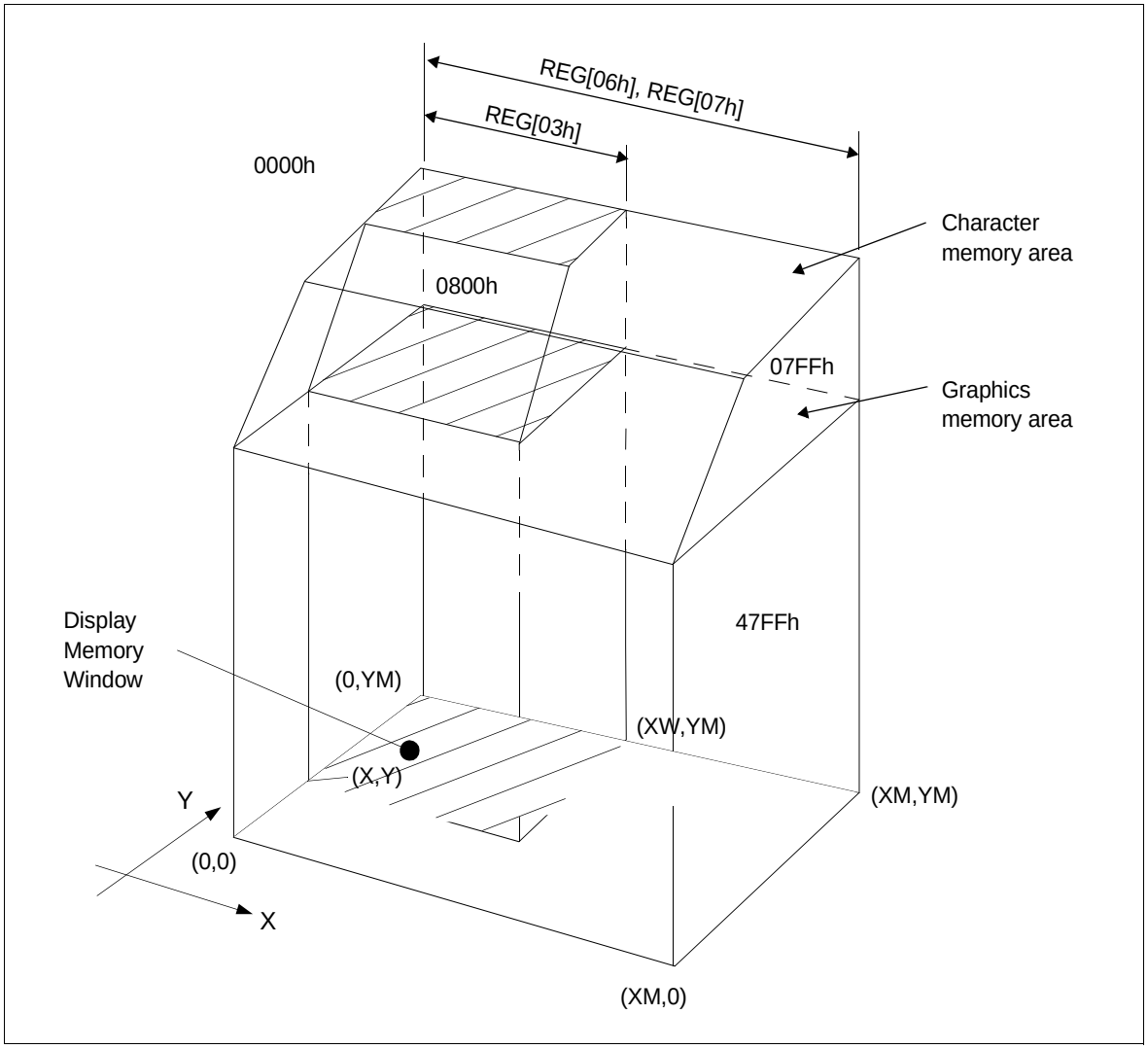


Figure 12-3 Virtual and Physical Screen Relationship

12.2.2 Display Address Scanning

The S1D13700F01 scans the display memory in the same way as a raster scan CRT screen. Each row is scanned from left to right until the address range equals C/R, REG[03h] bits 7-0. Rows are scanned from top to bottom. When in graphics mode, at the start of each line the address counter is set to the address at the start of the previous line plus the horizontal address range (or address pitch), REG[06h] - REG[07h].

In text mode, the address counter is set to the same start address, and the same character data is read, for each row in the character bitmap. However, a new row of the character generator output is used each time. Once all the rows in the character bitmap have been displayed, the address counter is set to the start address plus the horizontal address range (or address pitch) and the next line of text is displayed.

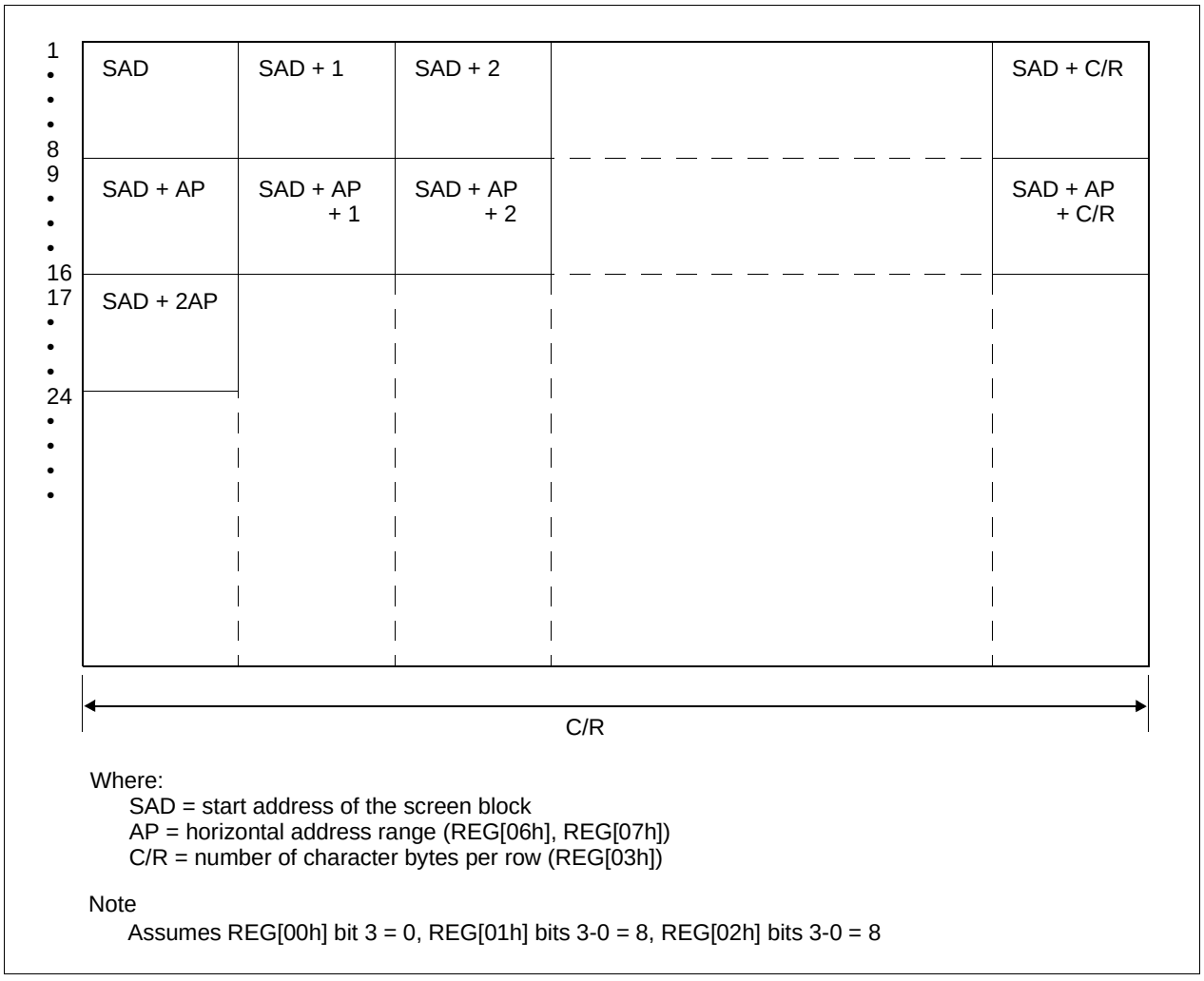


Figure 12-4 Display Addressing in Text Mode Example

Note
One byte of display memory corresponds to one character.

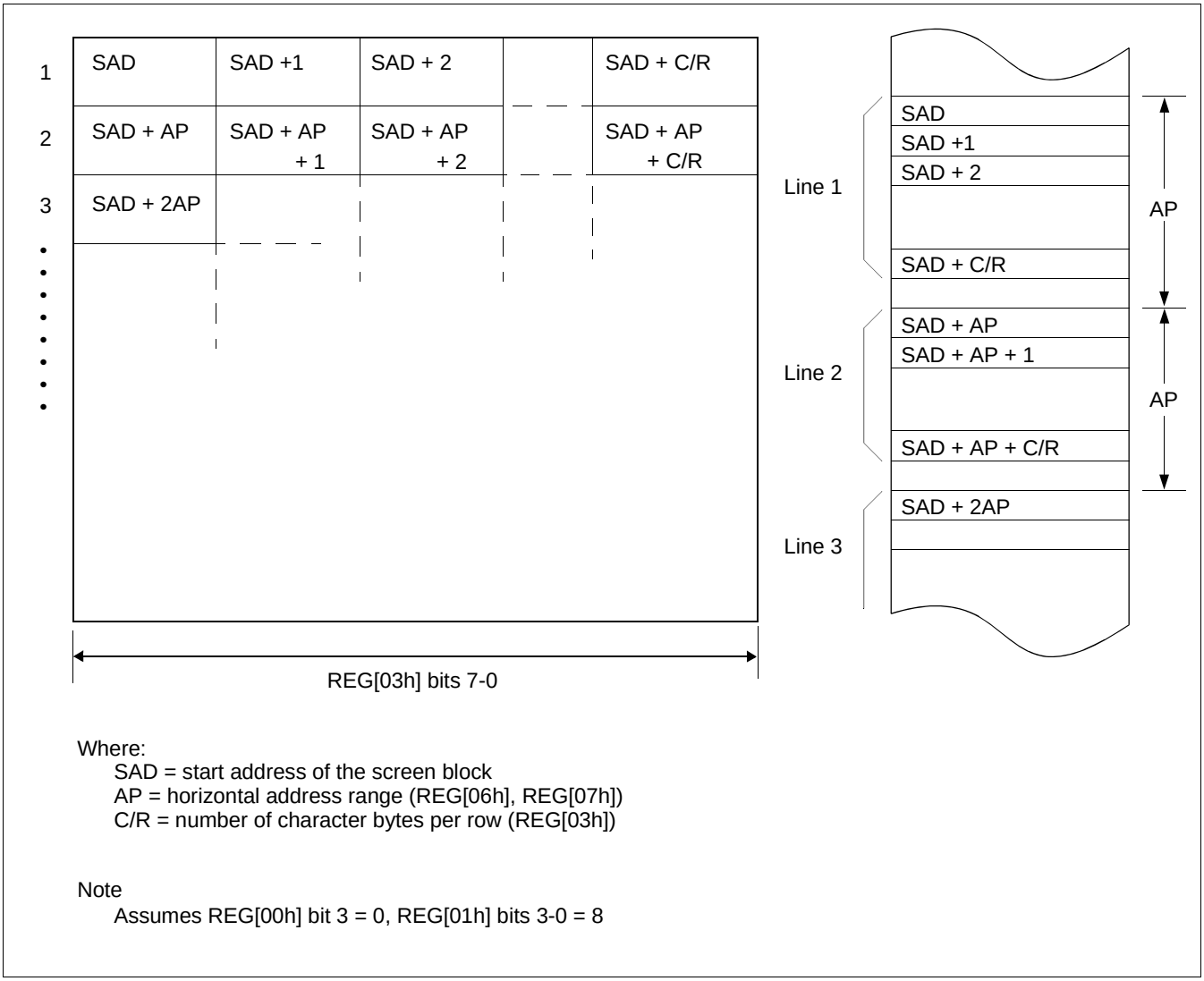
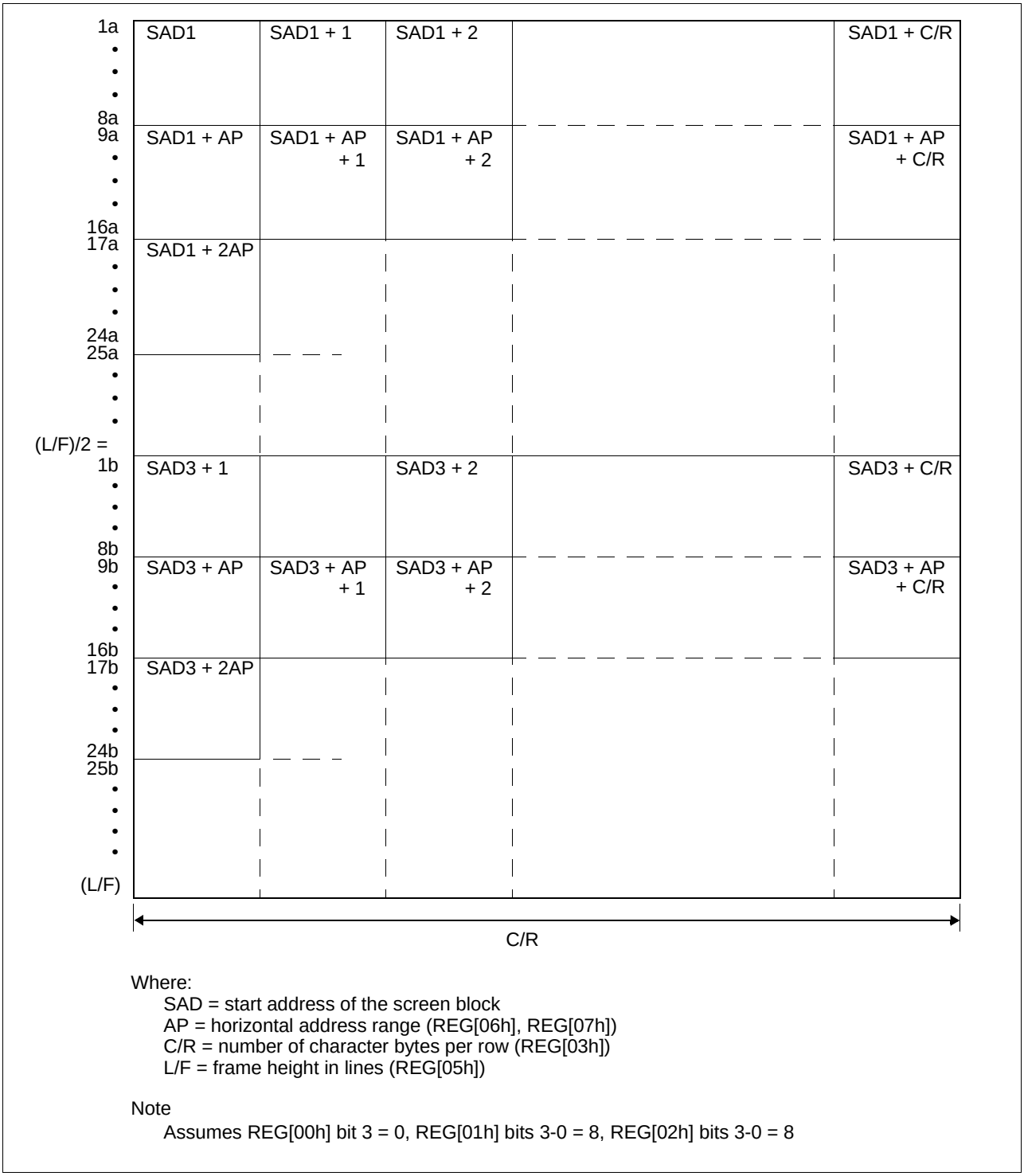


Figure 12-5 Display Addressing in Graphics Mode Example

Note

In 1 bpp, one bit of display memory corresponds to one pixel. Therefore, 1 byte of display memory corresponds to 8 pixels. In 2 bpp, 1 byte corresponds to 4 pixels. In 4 bpp, 1 byte corresponds to 2 pixels.



Where:
SAD = start address of the screen block
AP = horizontal address range (REG[06h], REG[07h])
C/R = number of character bytes per row (REG[03h])
L/F = frame height in lines (REG[05h])

Note
Assumes REG[00h] bit 3 = 0, REG[01h] bits 3-0 = 8, REG[02h] bits 3-0 = 8

Figure 12-6 Dual Panel Display Address Indexing in Text Mode

Note

In dual panel drive, the S1D13700F01 reads line 1a and line 1b as one cycle. The upper and lower panels are thus read alternately, one line at a time.

12.2.3 Display Scan Timing

During display scanning, the S1D13700F01 pauses at the end of each line for TC/R - C/R ((REG[04h] bits 7-0) - (REG[03h] bits 7-0)) display memory read cycles, although the LCD drive signals are still generated. TC/R may be set to any value within the constraints imposed by C/R, Input Clock (CLK), f_{FR}, and the size of the LCD panel. This pause may be used to fine tune the frame frequency.

Note

In text mode (when the CGROM or CGRAM is used), it is recommended that the microprocessor access the memory only during the pause at the end of each line (see Section 7.3.6, "Display Memory Access Timing for Text Mode" on page 36). Otherwise, flickering on the display may result during memory accesses.

For graphics mode, memory can be accessed at any time.

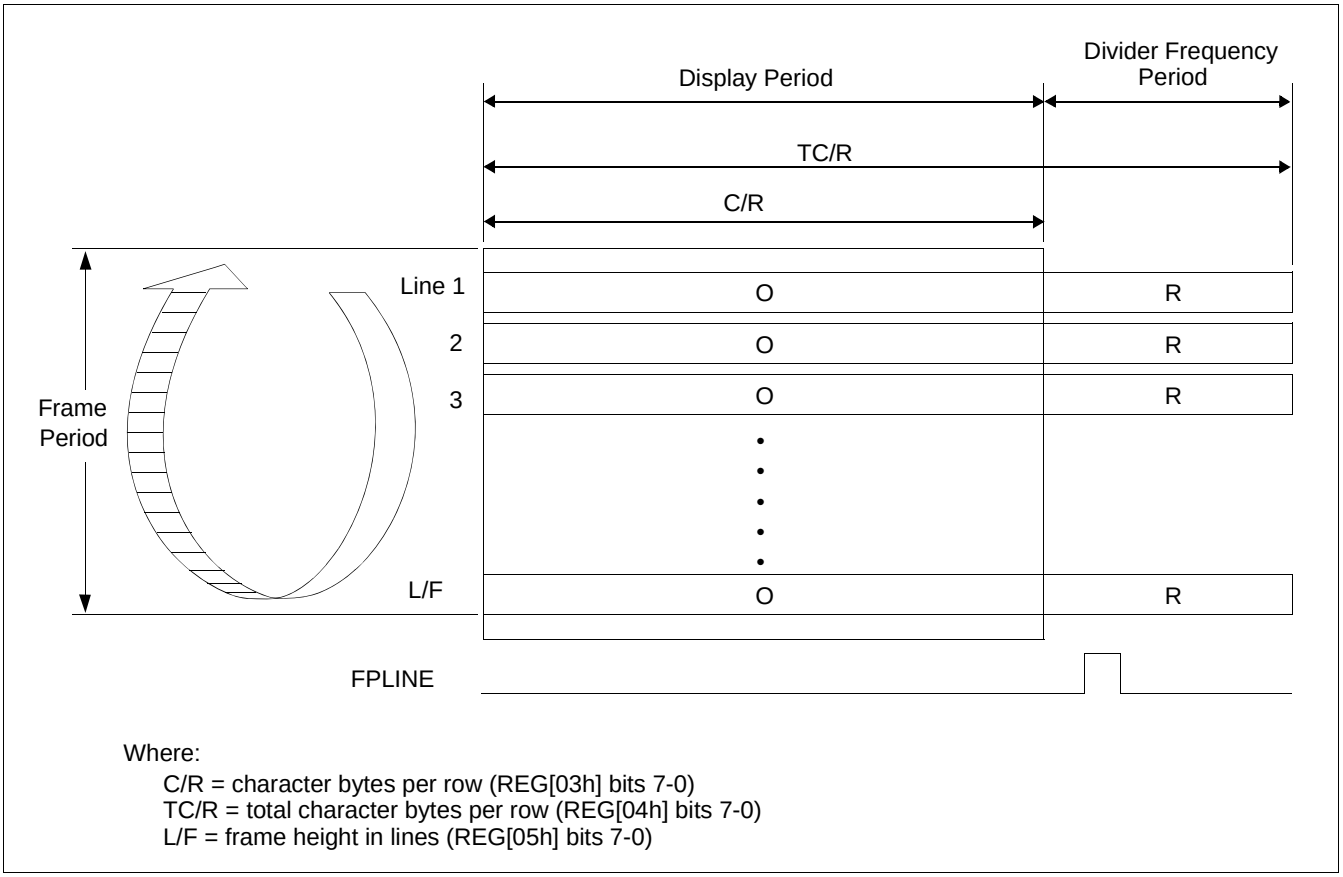


Figure 12-7 Relationship Between Total Character Bytes Per Row and Character Bytes Per Row

Note

The divider adjustment interval (R) applies to both the upper and lower screens even if a dual panel drive is selected, REG[00h] bit 3 = 1. In this case, FPLINE is active only at the end of the lower screen's display interval.

12.3 Cursor Control

12.3.1 Cursor Write Register Function

The Cursor Write register (REG[1Ch] - REG[1Dh]) functions as both the displayed cursor position address register and, in indirect addressing mode, the display memory access address register. When accessing display memory outside the actual visible screen memory, the Cursor Write register should be saved before accessing the memory and then restored after the memory access is complete. This is done to prevent the cursor from visibly disappearing outside the display area.

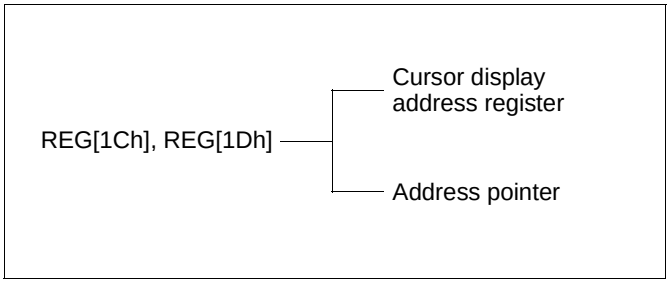


Figure 12-8 Cursor Addressing

Note
The cursor may disappear from the display if the cursor address remains outside the displayed screen memory for more than a few hundred milliseconds.

12.3.2 Cursor Movement

On each memory access, the Cursor Write register (REG[1Ch] - REG[1Dh]) is changed by the amount specified by the CSRDIR command (see REG[17h] bits 1-0) which automatically moves the cursor to the desired location.

12.3.3 Cursor Display Layers

Although the S1D13700F01 can display up to three layers, the cursor is displayed in only one of these layers. For a two layer configuration (REG[18h] bit 4 = 0), the cursor is displayed in the first layer (L1). For a three layer configuration (REG[18h] bit 4 = 1), the cursor is displayed in the third layer (L3).

The cursor is not displayed if the address is moved outside of the memory for its layer. If it is necessary to display the cursor in a layer other than the present one, the layers may be swapped, or the cursor layer can be moved within the display memory.

Although the cursor is normally displayed for character data, the S1D13700F01 may also display a dummy cursor for graphical characters. This is only possible if a graphics screen is displayed, the text screen is turned off, and the microprocessor generates the cursor control address.

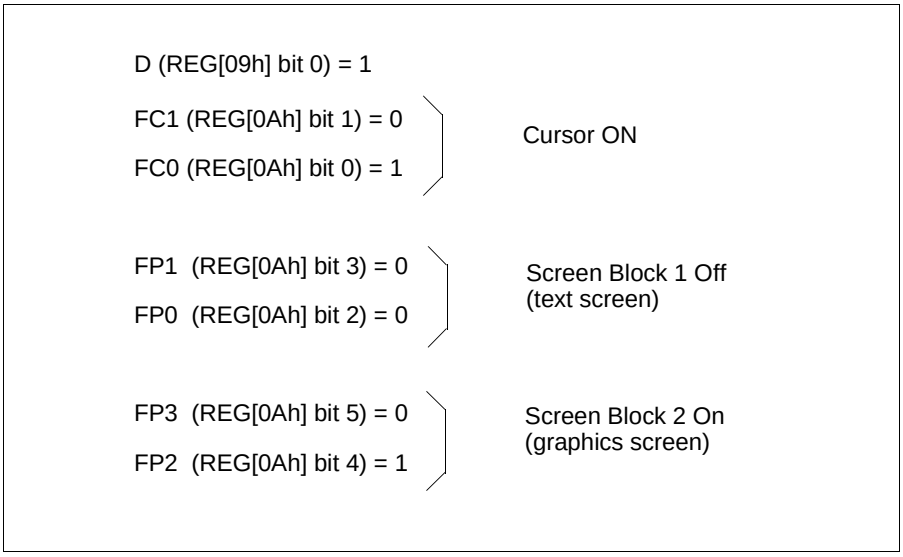


Figure 12-9 Cursor Display Layers

For example, if Chinese characters are displayed on a graphics screen, the cursor address is set to the second screen block in order to write the “graphics” display data. However, the cursor is not displayed. To display the cursor, the cursor address must be set to an address within the blank text screen block.

Since the automatic cursor increment is in address units, not character units, the controlling microprocessor must set the Cursor Write register (REG[1Ch] - REG[1Dh]) when moving the cursor over the graphical characters.

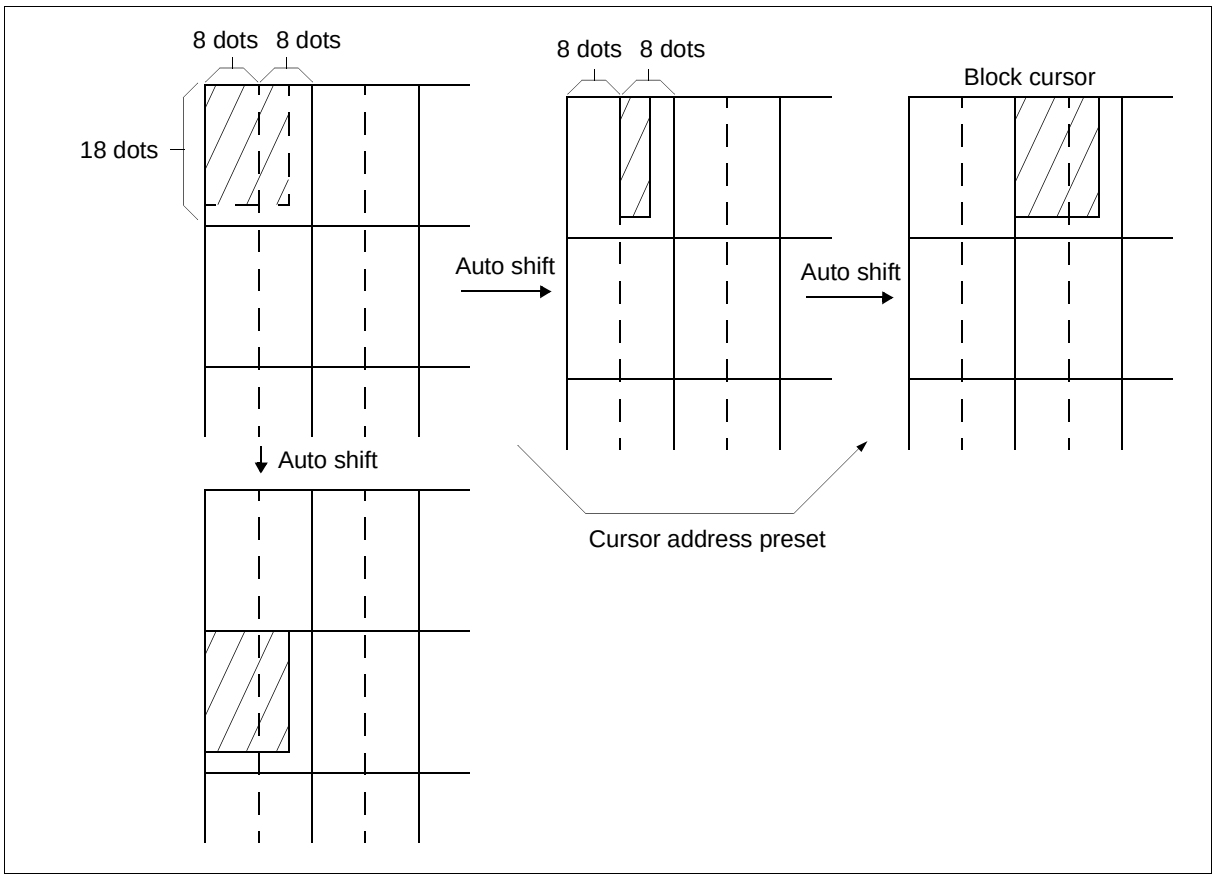


Figure 12-10 Cursor Movement

If no text screen is displayed, only a bar cursor can be displayed at the cursor address.

If the first layer is a mixed text and graphics screen and the cursor shape is set to a block cursor, the S1D13700F01 automatically decides which cursor shape to display. On the text screen it displays a block cursor, and on the graphics screen, a bar cursor.

12.4 Memory to Display Relationship

The S1D13700F01 supports virtual screens that are larger than the physical size of the LCD panel address range (C/R), REG[03h] bits 7-0. A layer of the S1D13700F01 can be considered as a window into the larger virtual screen held in display memory. This window can be divided into two blocks, with each block able to display a different portion of the virtual screen.

For example, this allows one block to dynamically scroll through a data area while the other block is used as a status message display area.

For examples of the memory to display relationships, see Figure 12-11 “Screen Layers and Memory Relationship,” on page 87 and Figure 12-12 “Virtual Display (Display Window to Memory Relationship),” on page 88, and Figure 12-13 “Memory Map and Magnified Characters,” on page 89.

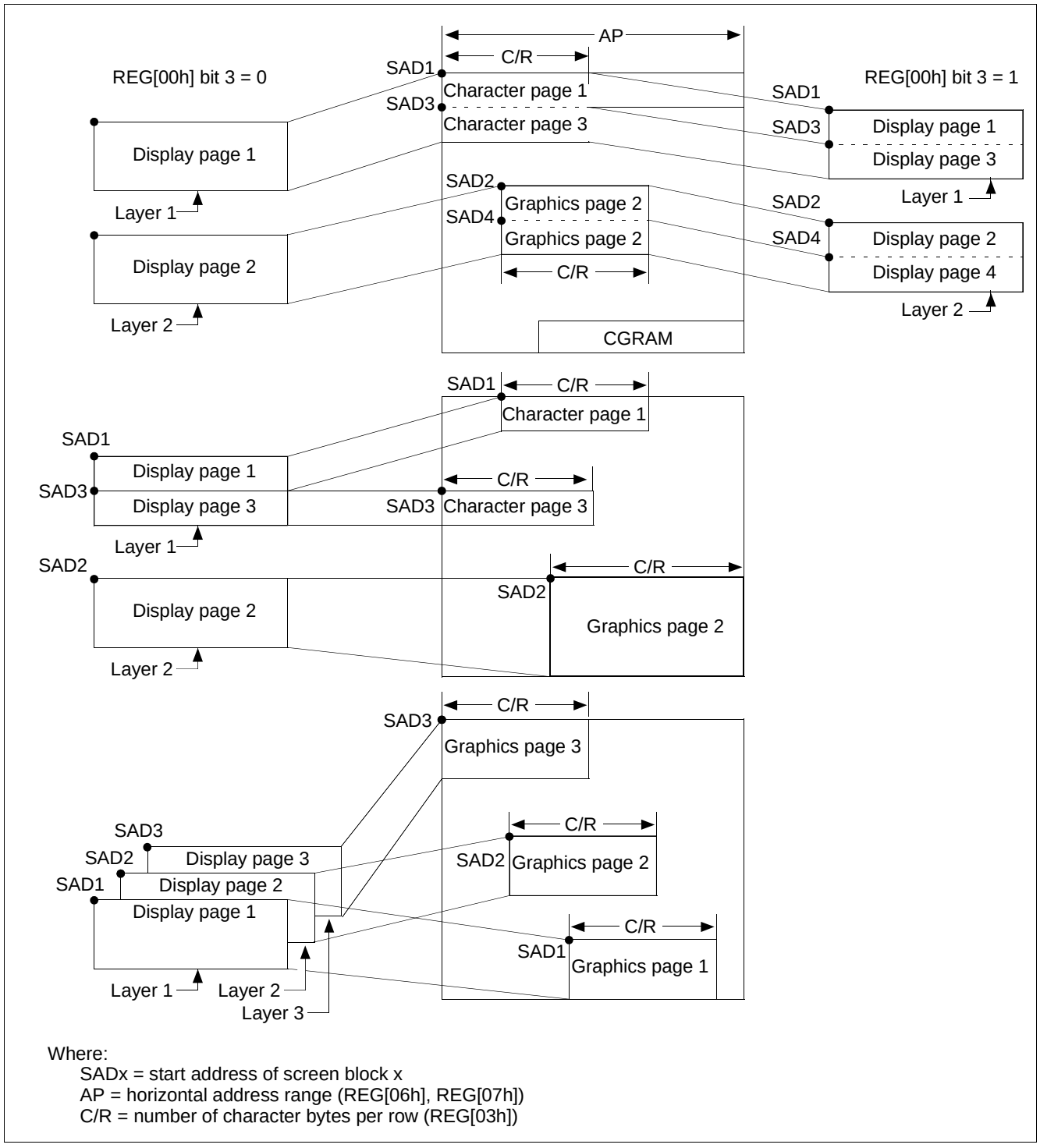


Figure 12-11 Screen Layers and Memory Relationship

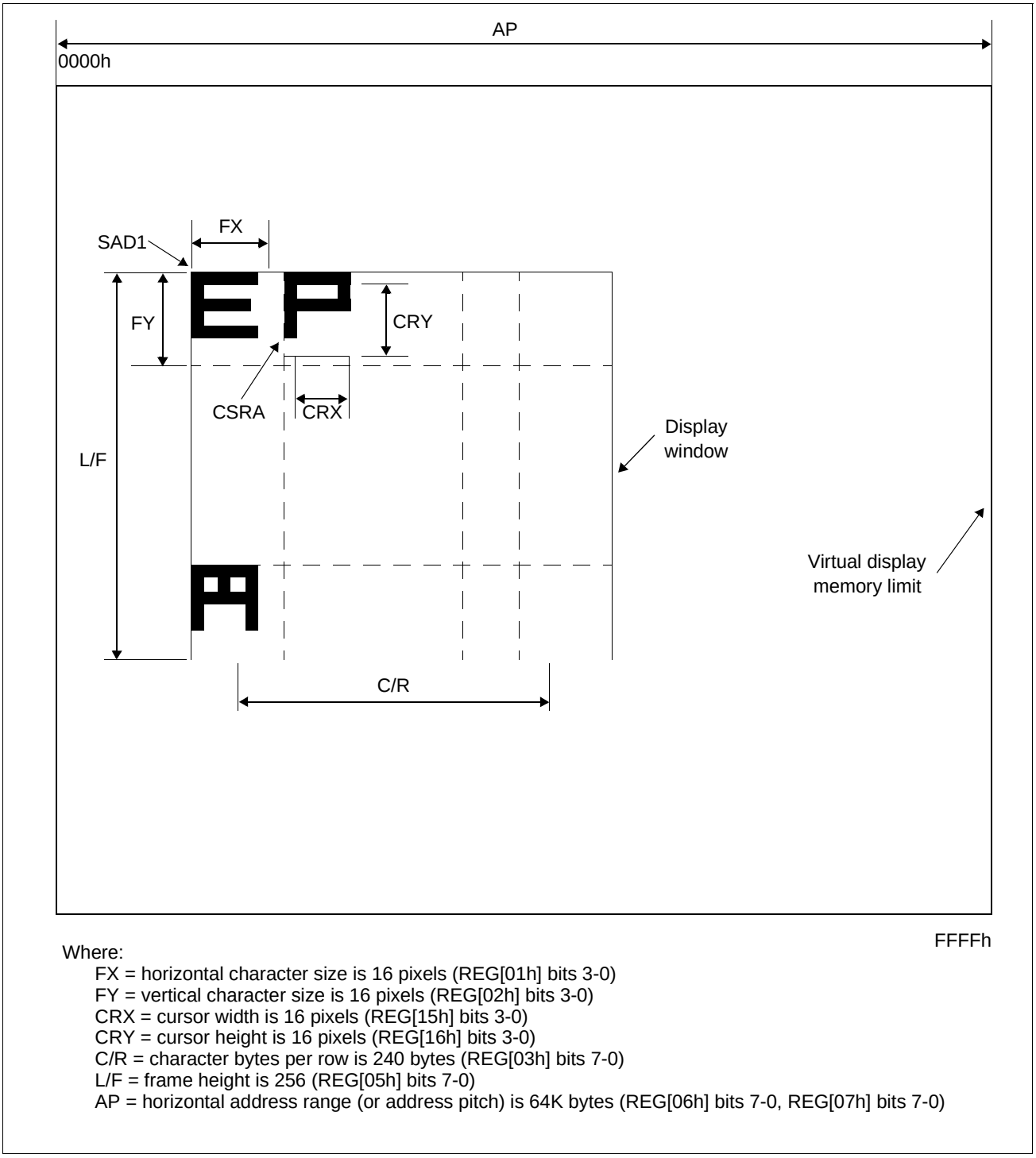


Figure 12-12 Virtual Display (Display Window to Memory Relationship)

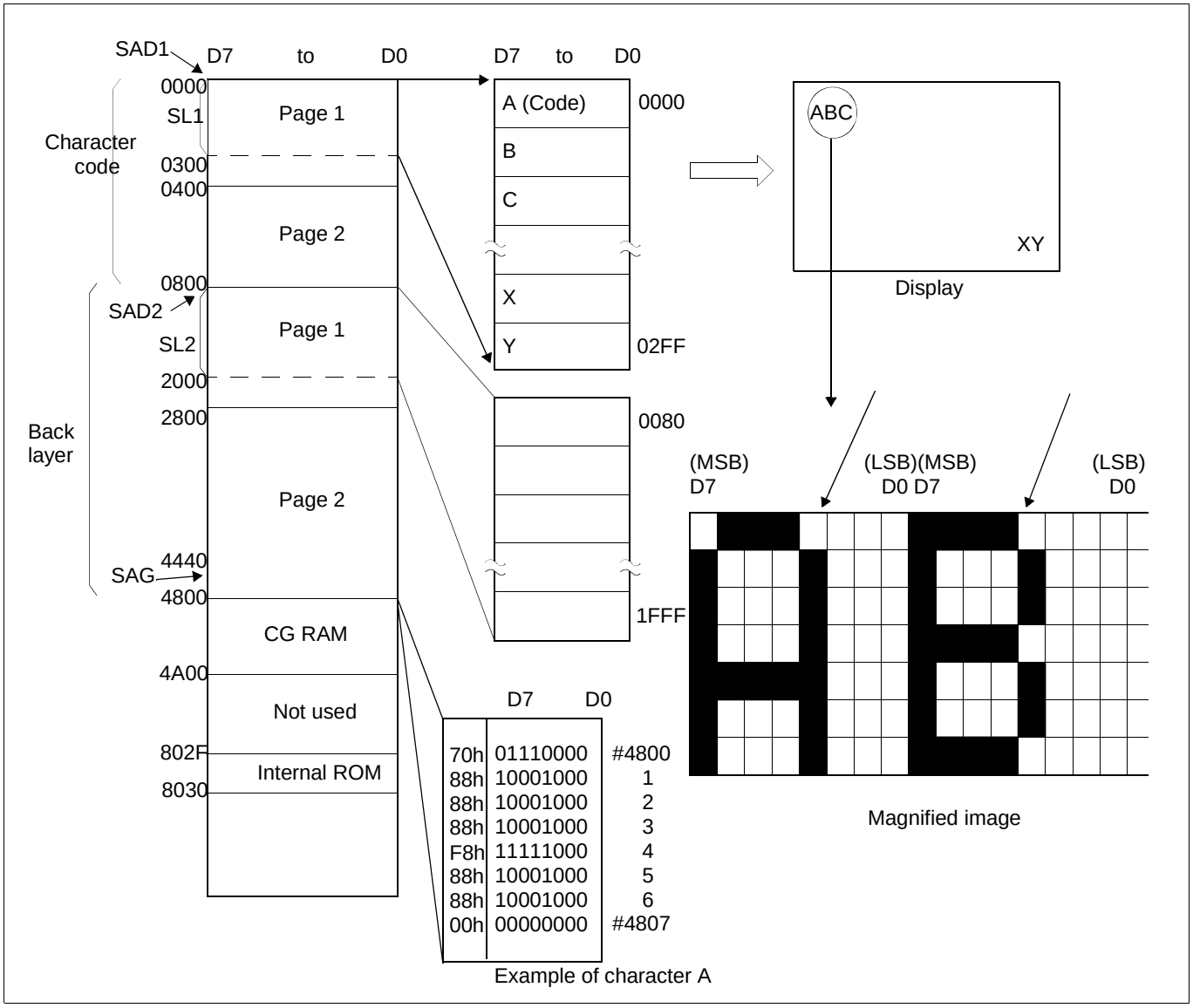


Figure 12-13 Memory Map and Magnified Characters

12.5 Scrolling

The microprocessor can control S1D13700F01 scrolling modes by writing the scroll address registers for each screen block, REG[0Bh] - REG[14h]. This is referred to as address scrolling and can be used for both text and graphic screen blocks, if the display memory capacity is greater than one screen.

12.5.1 On-Page Scrolling

The normal method of scrolling within a page is to move the whole display up one line and erase the bottom line. However, the S1D13700F01 does not automatically erase the bottom line, so it must be erased with blanking data when changing the scroll address register.

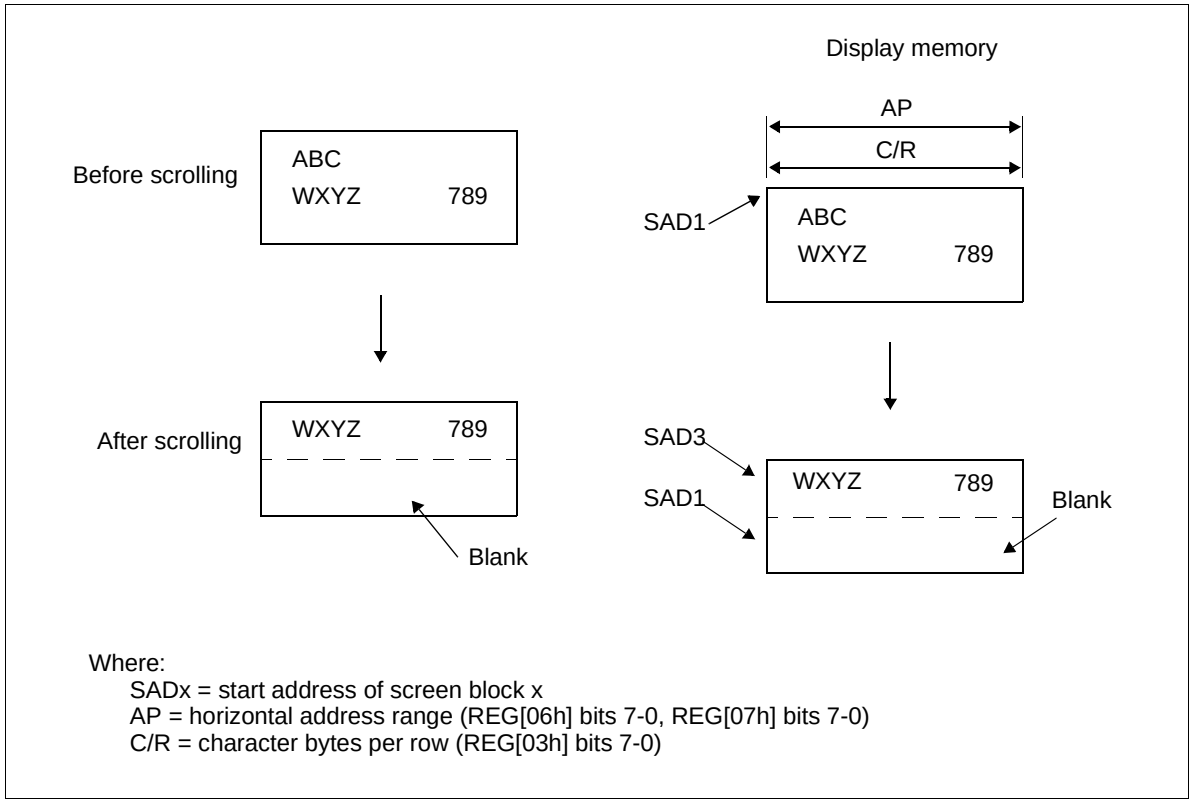


Figure 12-14 On-Page Scrolling

12.5.2 Inter-Page Scrolling

Scrolling between pages and page switching can be performed only if the display memory capacity is greater than one screen. To scroll down one line/character, add the value of the horizontal address range (or address pitch), REG[06h] - REG[07h], to the current SADx. To scroll up, subtract the value of the horizontal address range from SADx.

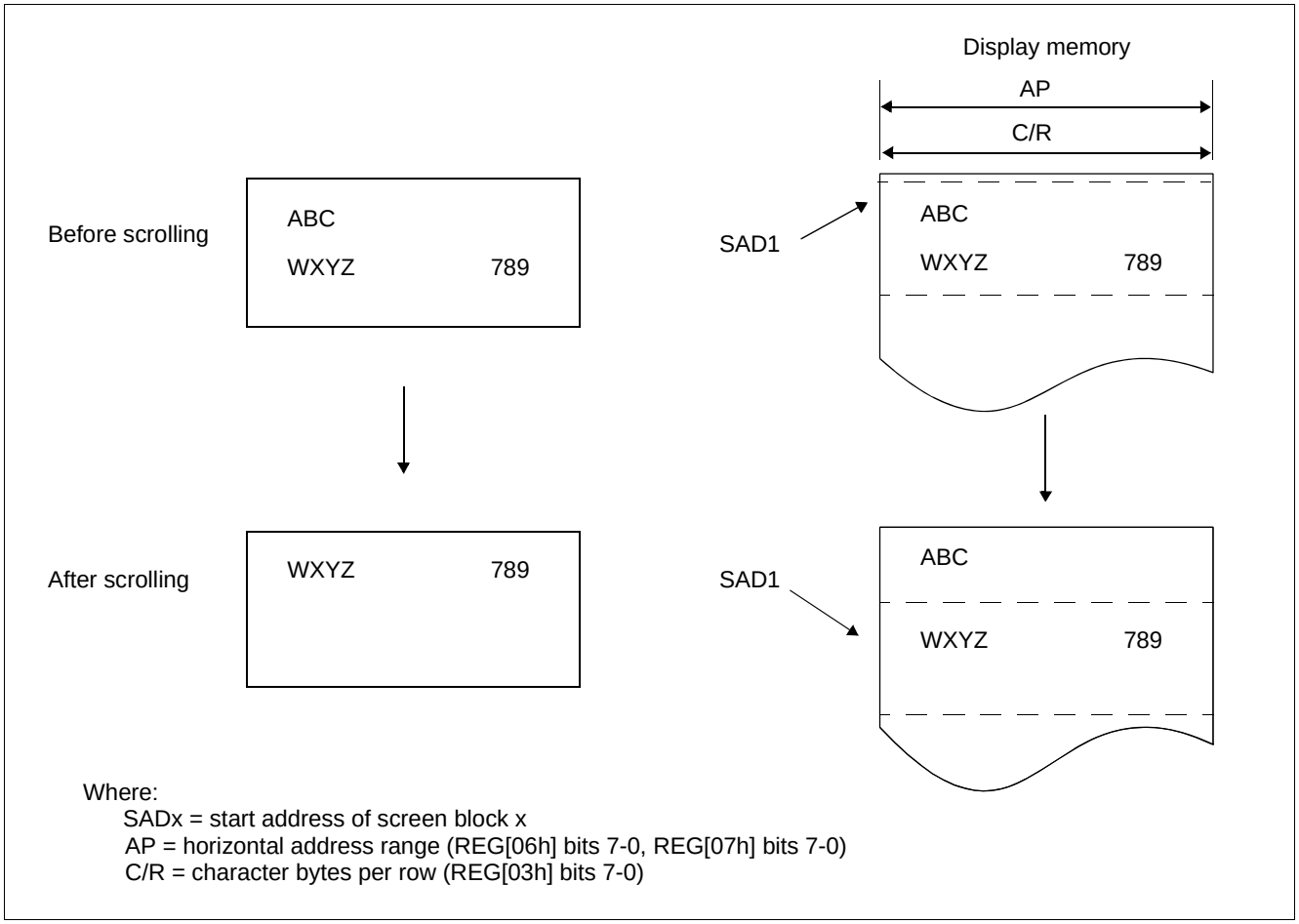


Figure 12-15 Inter-Page Scrolling

12.5.3 Horizontal Wraparound Scrolling

For screen block in text mode, the display can be scrolled horizontally in one character units, regardless of the display memory capacity.

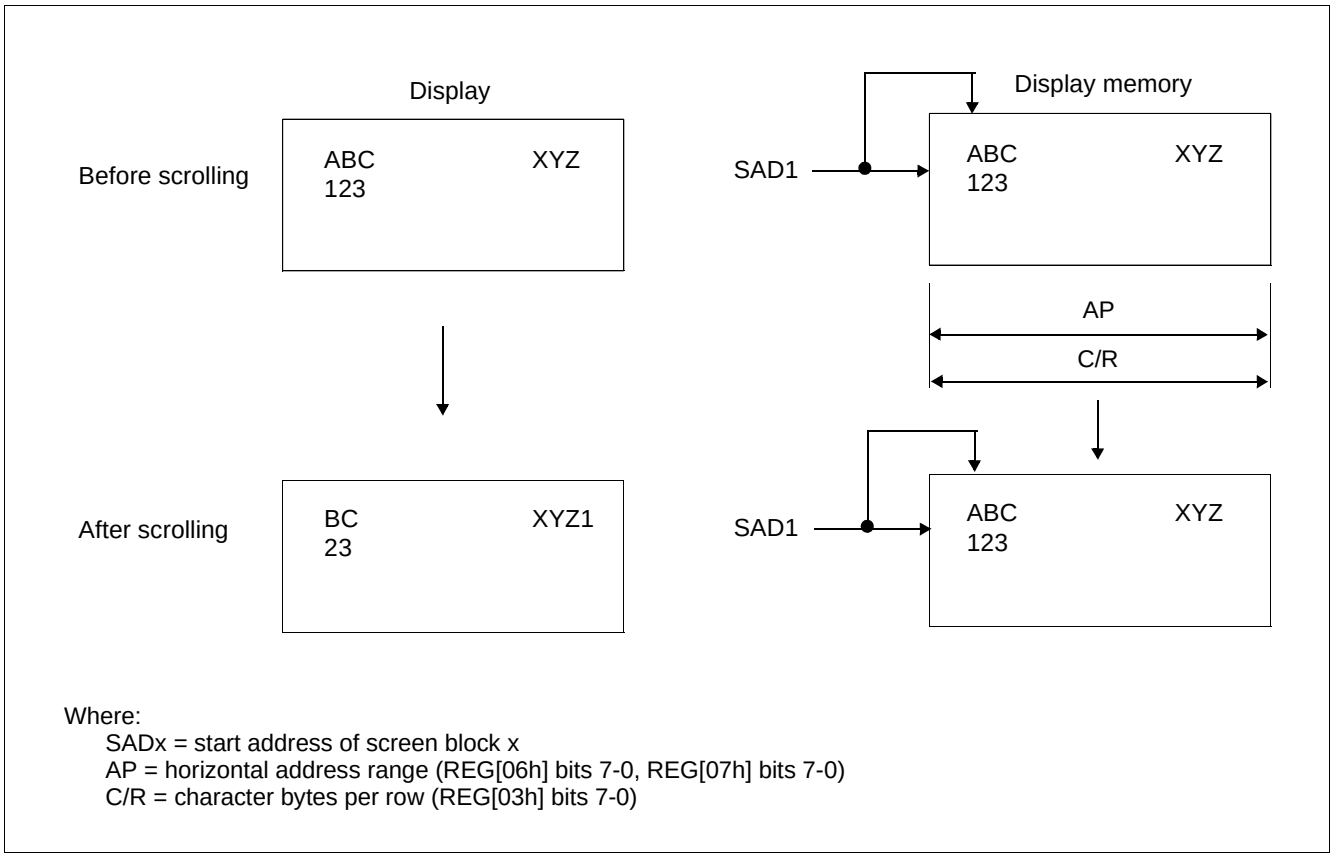


Figure 12-16 Horizontal Wraparound Scrolling

12.5.4 Bi-directional Scrolling

Bi-directional scrolling can be performed only if the display memory is larger than the physical screen in both the horizontal (REG[06h], REG[07h] > REG[03h]) and vertical directions. Scrolling is normally done in single-character units, however the HDOT SCR command (see REG[1Bh] bits 2-0) allows horizontal scrolling in pixel units (for text blocks only). Single pixel horizontal scrolling can be performed using both the SCROLL and HDOT SCR commands. For more information, see Section 15.3, “Smooth Horizontal Scrolling” on page 115.

Note

In 2 bpp and 4 bpp grayscale mode REG[1Bh] bits 2-0 (HDOT SCR) must be set to 0, so horizontal scrolling can only be done in single character units (not pixel units).

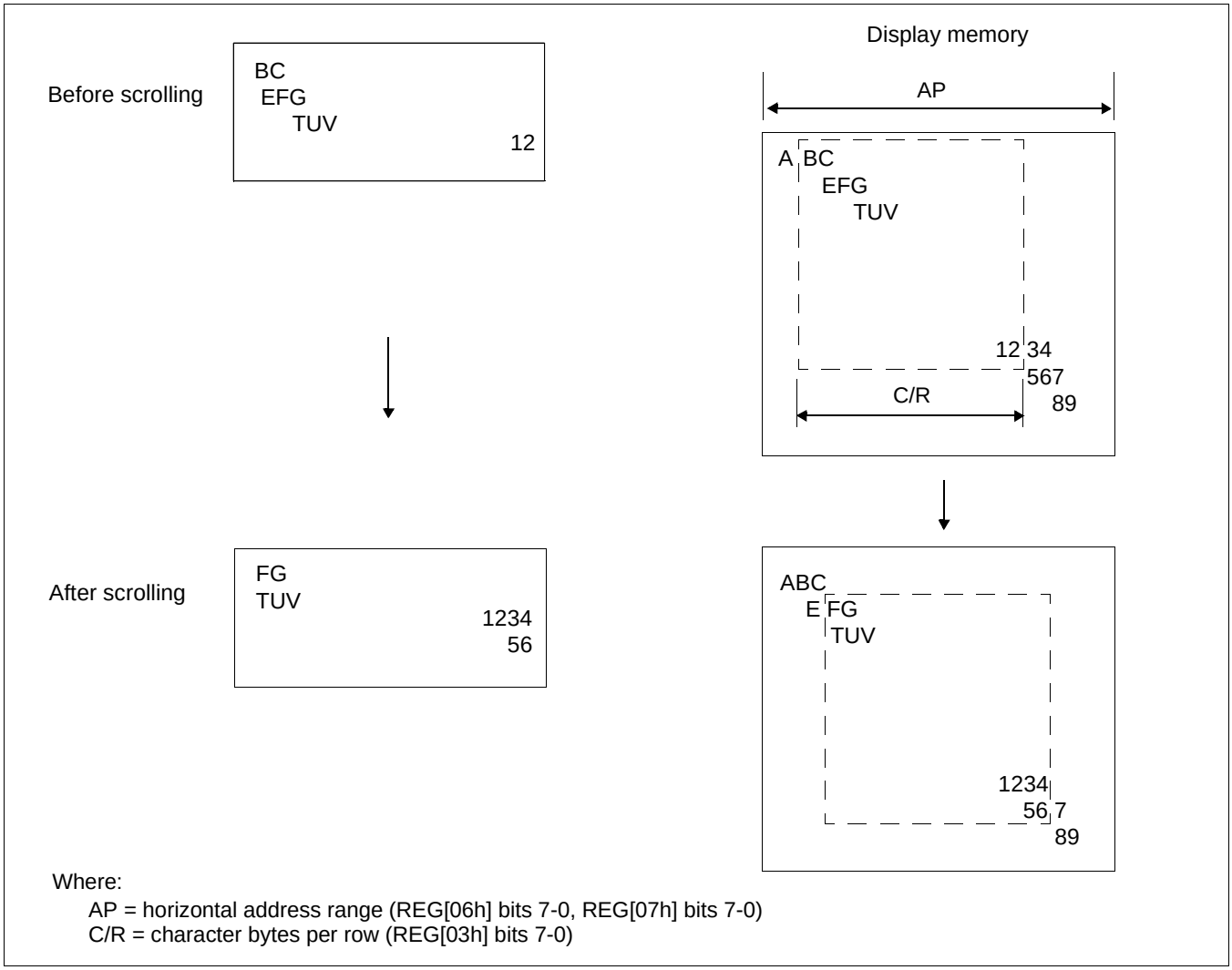


Figure 12-17 Bi-Directional Scrolling

12.5.5 Scroll Units

The following table summarizes the units, or steps, that can be scrolled for each mode.

Table 12-1 Scrolling Unit Summary

Mode	Vertical	Horizontal
Text	Characters	Pixels or Characters
Graphics	Pixels	Pixels

Note

In a divided screen, each block cannot be independently scrolled horizontally in pixel units.

13 Character Generator

13.1 CG Characteristics

13.1.1 Internal Character Generator

The internal character generator is recommended for minimum system configurations containing a S1D13700F01, display RAM, LCD panel, single-chip microprocessor and power supply. Since the internal character generator uses a CMOS mask ROM, it is also recommended for low-power applications.

- 5 x 7 pixel font (See Section 16, “Internal Character Generator Font” on page 124)
- 160 JIS standard characters
- Can be mixed with character generator RAM (maximum of 64 CGRAM characters)
- Can be automatically spaced out up to 8 x 16 pixels

13.1.2 Character Generator RAM

The character generator RAM can be used for storing graphics characters. The character generator RAM can be mapped to any display memory location by the microprocessor, allowing effective usage of unused address space.

- Up to 8 x 8 pixel characters when REG[00h] bit 2 = 0 and 8 x 16 characters when REG[00h] bit 2 = 1
- Can be mapped anywhere in display memory address space if used with the character generator ROM (REG[00h] bit 0 = 0)

Note
If the CGRAM is used (includes CGRAM1 and CGRAM2), only 1 bpp is supported.

13.2 Setting the Character Generator Address

The CGRAM addresses in the display memory address space are not mapped directly from the address in the Character Generator RAM Start Address registers, REG[19h] - REG[1Ah]. The data to be displayed is at a CGRAM address calculated from (REG[19h] - REG[1Ah]) + character code + ROW select address. For the ROW select address, see Figure 13-1 “Row Select Address,” on page 97.

The following tables show the address mapping for CGRAM addresses.

Table 13-1 Character Fonts Where Number of Lines ≤ 8 (REG[00h] bit 2 = 0)

SAG	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Character Code	0	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0
+ROW Select Address	0	0	0	0	0	0	0	0	0	0	0	0	0	R2	R1	R0
CGRAM Address	VA15	VA14	VA13	VA12	VA11	VA10	VA9	VA8	VA7	VA6	VA5	VA4	VA3	VA2	VA1	VA0

Table 13-2 Character Fonts Where Number of Lines ≤ 16 (REG[00h] bit 2 = 1)

SAG	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Character Code	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0	0
+ROW Select Address	0	0	0	0	0	0	0	0	0	0	0	0	R3	R2	R1	R0
CGRAM Address	VA15	VA14	VA13	VA12	VA11	VA10	VA9	VA8	VA7	VA6	VA5	VA4	VA3	VA2	VA1	VA0

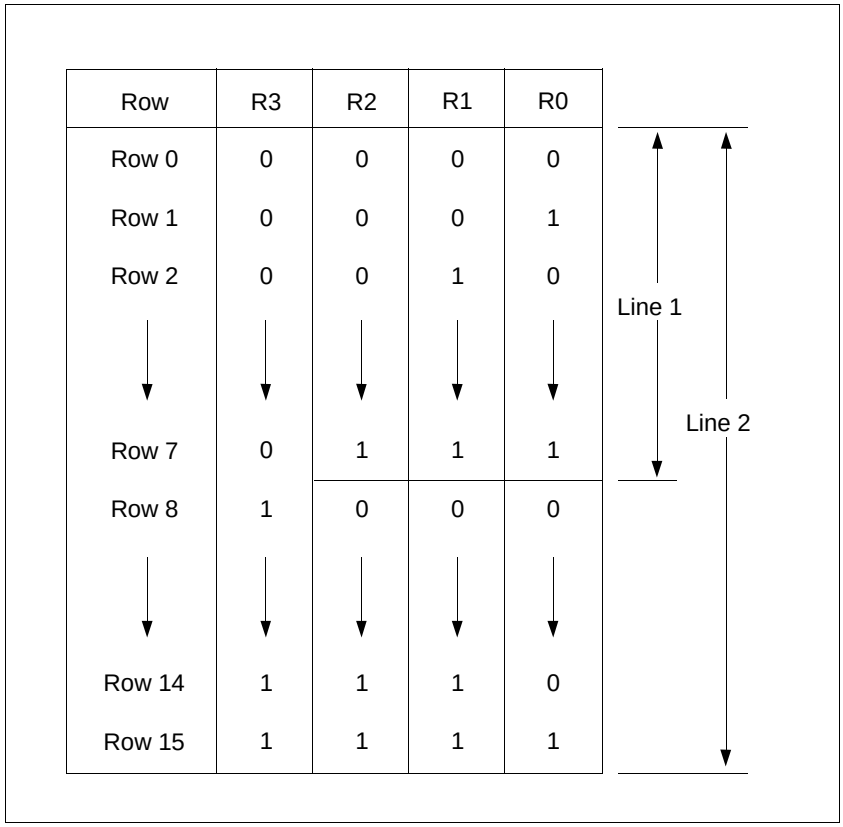


Figure 13-1 Row Select Address

Note

Lines = 1: lines in the character bitmap ≤ 8.
Lines = 2: lines in the character bitmap ≥ 9.

13.2.1 CGRAM Addressing Example

Example 1: Define a pattern for the "A" in Figure 12-1 on page 77. The CGRAM table start address is 4800h. The character code for the defined pattern is 80h (the first character code in the CGRAM area).

As the character codes in Figure 13-2 "On-Chip Character Codes," on page 99 show, codes 80h to 9Fh and E0h to FFh are allocated to the CGRAM and can be used as desired. 80h is the first code for the CGRAM. As characters cannot be used if only using graphics mode, there is no need to set the CGRAM data.

Table 13-3 Character Data Example

CGRAM ADR	5Ch	Reverse the CGRAM address calculation to calculate SAG
P1	00h	
P2	40h	
CSRDIR	4Ch	Set cursor shift direction to right
CSRW	46h	CGRAM start address is 4800h
P1	00h	
P2	48h	
MWRITE	42h	
P	70h	Write ROW 0 data
P2	88h	Write ROW 1 data
P3	88h	Write ROW 2 data
P4	88h	Write ROW 3 data
P5	F8h	Write ROW 4 data
P6	88h	Write ROW 5 data
P7	88h	Write ROW 6 data
P8	00h	Write ROW 7 data
P9	00h	Write ROW 8 data
↓	↓	↓
P16	00h	Write ROW 15 data

13.3 Character Codes

The following figure shows the character codes and the codes allocated to CGRAM. All codes can be used by the CGRAM if not using the internal ROM, but the CGRAM address must be set to 0.

Note
If either of CGRAM1 or CGRAM2 are used, only 1 bpp is supported.

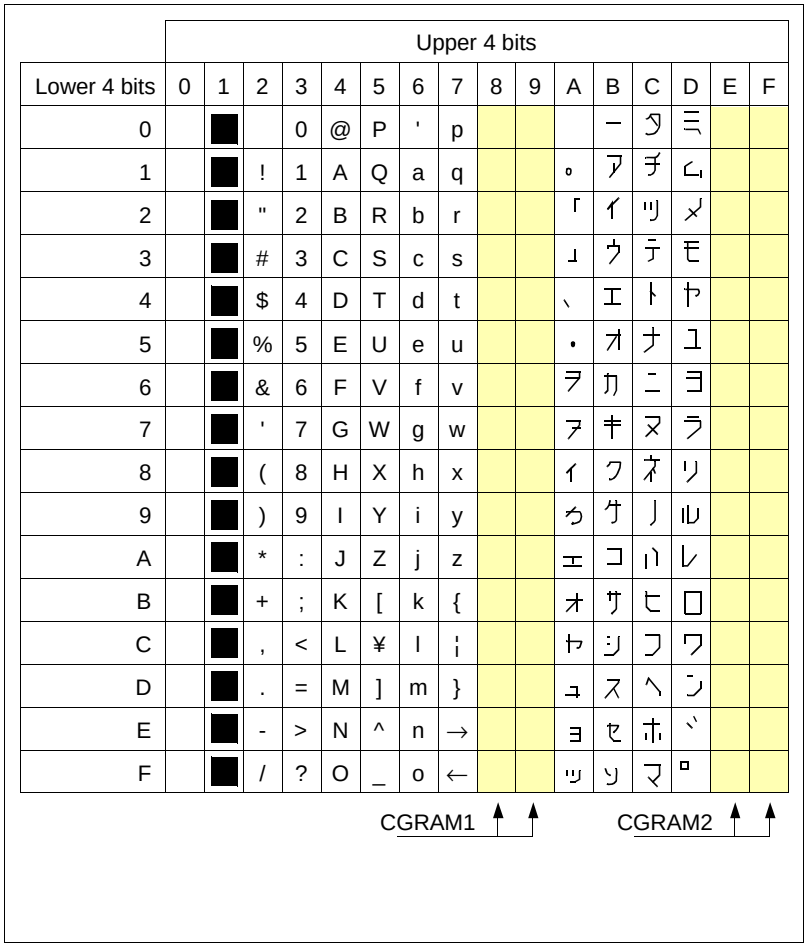


Figure 13-2 On-Chip Character Codes

14 Microprocessor Interface

14.1 System Bus Interface

CNF[4:0], A[15:1], A0, D[7:0], RD#, WR#, AS and CS are used as control signals for the microprocessor data bus. A0 is normally connected to the lowest bit of the system address bus. CNF[4:2] change the operation of the RD# and WR# pins to enable interfacing to either a Generic (Z80), M6800, or MC68K family bus, and should be pulled-up or pulled-down according to Table 5-6: “Summary of Configuration Options,” on page 20.

14.1.1 Generic

The following table shows the signal states for each function.

Table 14-1 Generic Interface Signals

A0	RD#	WR#	Function
1	0	1	Display data and cursor address read
0	1	0	Display data and parameter write
1	1	0	Command write

14.1.2 M6800 Family

The following table shows the signal states for each function.

Table 14-2 M6800 Family Interface Signals

A0	R/W#	E	Function
1	1	1	Display data and cursor address read
0	0	1	Display data and parameter write
1	0	1	Command write

14.1.3 MC68K Family

The following table shows the signal states for each function.

Table 14-3 MC68K Family Interface Signals

A0	RD/WR#	LDS#	Function
1	1	0	Display data and cursor address read
0	0	0	Display data and parameter write
1	0	0	Command write

15 Application Notes

15.1 Register Initialization/Initialization Parameters

Square brackets around a parameter name indicate the number represented by the parameter, rather than the value written to the parameter register. For example, [FX] = FX + 1.

15.1.1 SYSTEM SET Command and Parameters

- FX
  The horizontal character field size is determined from the horizontal display size in pixels [VD] and the number of characters per line [VC].

  [VD] ÷ [VC] = [FX]

- C/R

  C/R can be determined from VC and FX.

  [C/R] = RNDUP ([FX] ÷ 8) [VC]

  Where RNDUP(x) denotes rounded up to the next highest integer. [C/R] is the number of bytes per line, not the number of characters.

- TC/R

  TC/R must satisfy the condition [TC/R] ≥ [C/R] + 2.

- L/F

  The number of lines per frame is determined by the display vertical resolution.

- f_{SYSCLK} and f_{FR}

  Once TC/R has been set, the frame frequency, f_{FR}, and lines per frame [L/F] will also have been set. Depending on number of gray shades (bpp) selected and the horizontal character field size, [FX], the oscillator frequency f_{SYSCLK} is given by one of the following formula:

For 1 Bpp and [FX] ≥ 8:

f_{SYSCLK} = 2 x [ClockDiv] x Ffr x [L/F] x F (Hz)

where
A = [TC/R] - [C/R]
B = RNDDN([C/R] x [FX] ÷ 8)
C = 16 x RNDUP(B ÷ 16)
D = C - B
E = (B x 16 ÷ [FX] + D) ÷ 2

F = A + E

For 1 Bpp and [FX] < 8:

f_{SYSCLK} = 2 x [ClockDiv] x Ffr x [L/F] x F (Hz)

where
A = [TC/R] - [C/R]
B = RNDDN([C/R] x [FX] ÷ 4)
C = 16 x RNDUP(B ÷ 16)
D = C - B
E = (B x 8 ÷ [FX] + D) ÷ 2
F = A + E

For 2 Bpp:

f_{SYSCLK} = 2 x [ClockDiv] x Ffr x [L/F] x (A + C +1) (Hz)

where
A = [TC/R] - [C/R] + 1
B = RNDDN([C/R] x [FX] ÷ 8)
C = 16 x RNDUP(B ÷ 16)

For 4 Bpp:

f_{SYSCLK} = 2 x [ClockDiv] x Ffr x [L/F] x (A + 2 x C + 2) (Hz)

where
A = [TC/R] - [C/R] + 2
B = RNDDN([C/R] x [FX] ÷ 16)
C = 16 x RNDUP(B ÷ 16)

For all cases above where:

ClockDiv	4, 8, or 16
Ffr	Frame Rate

If no standard crystal close to the calculated value of f_{SYSCLK} exists, a higher frequency crystal can be used and the value of TC/R revised using one of the above equations.

- Symptoms of an incorrect TC/R setting are listed below. If any of these appears, check the value of TC/R and modify it if necessary.
  - Vertical scanning halts and a high-contrast horizontal line appears.
  - All pixels are on or off.
  - The FPLINE output signal is absent or corrupted.
  - The display is unstable.

Table 15-1 Panel Calculations

Product Resolution (X × Y)	[FX]	[FY]	[C/R]	[TC/R]	f_{OSC} (MHz) See note 2
256 x 64	[FX] = 6 pixels: 256 ÷ 6 = 42 remainder 4 = 4 blank pixels	8 or 16, depending on the screen	[C/R] = 42 bytes. When using HDOT SCR, [C/R] = 43 bytes	46	1.66
512 x 64	[FX] = 6 pixels: 512 ÷ 6 = 85 remainder 2 = 2 blank pixels	8 or 16, depending on the screen	[C/R] = 85 bytes. When using HDOT SCR, [C/R] = 86 bytes	98	3.52
256 x 128	[FX] = 8 pixels: 256 ÷ 8 = 32 remainder 0 = no blank pixels	8 or 16, depending on the screen	[C/R] = 32 bytes. When using HDOT SCR, [C/R] = 33 bytes	36	2.5
512 x 128	[FX] = 10 pixels: 256 ÷ 10 = 51 remainder 2 = 2 blank pixels	8 or 16, depending on the screen	[C/R] = 102 bytes. When using HDOT SCR, [C/R] = 103 bytes	120	8.6

Note

[1] The remaining pixels on the right-hand side of the display are automatically blanked by the S1D13700F01. There is no need to zero the display memory corresponding to these pixels.

[2] Assumes a frame frequency of 70 Hz, 1 bpp, and a clock divide of 4.

15.1.2 Initialization Example

The initialization example shown below is for a S1D13700F01 with an 8-bit microprocessor interface bus and an Epson EG4810S-AR display unit (512 × 128 pixels).

Indirect Addressing

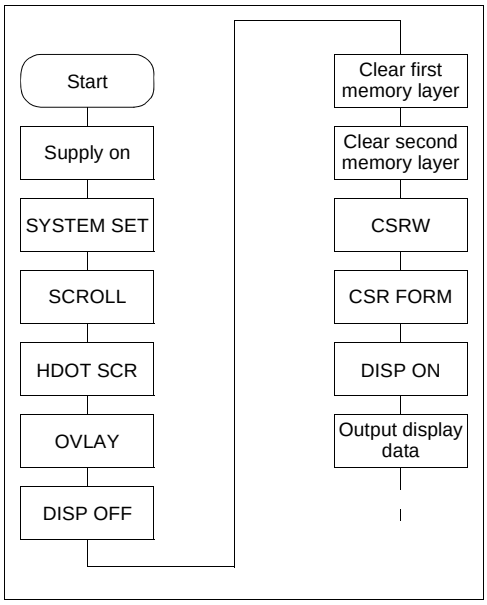


Figure 15-1 Initialization Procedure

Note

Set the cursor address to the start of each screen's layer memory, and use MWRITE to fill the memory with space characters, 20h (text screen only) or 00h (graphics screen only). Determining which memory to clear is explained in Section 15.1.3, "Display Mode Setting Example 1: Combining Text and Graphics" on page 109.

Table 15-2 Indirect Addressing Initialization Procedure

No.	Command	Operation
1	Power-up	
2	Supply	
3	SYSTEM SET	
	C = 40h	
	P1 = 38h	M0: Internal CGROM (REG[00h] bit 0)
		M2: 8 lines per character (REG[00h] bit 2)
		W/S: Two-panel drive (REG[00h] bit 3)
		IV: Sets top-line compensation to none (REG[00h] bit 5)
	P2 = 87h	FX: Horizontal character size = 8 pixels (REG[01h] bits 3-0)
		MOD: Two-frame AC drive (REG[01h] bit 7)

Table 15-2 Indirect Addressing Initialization Procedure (Continued)

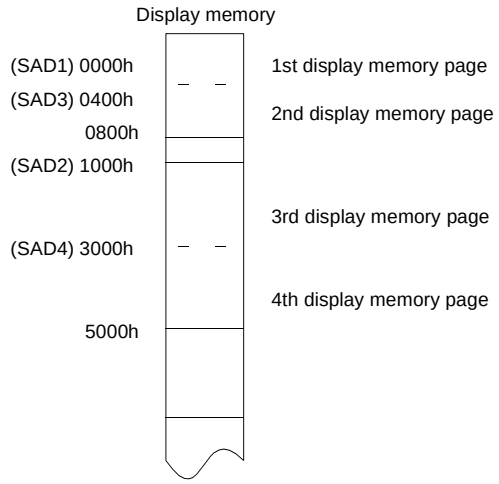
No.	Command	Operation
	P3 = 07h	FY: Vertical character size = 8 pixels (REG[02h] bits 3-0
	P4 = 3Fh	C/R: 64 display addresses per line (REG[03h] bits 7-0)
	P5 = 49h	TC/R: Total address range per line = 90 (REG[04h] bits 7-0)
		fOSC = 6.5 MHz, fFR = 70 Hz
	P6 = 7Fh	L/F: 128 display lines (REG[05h] bits 7-0
	P7 = 80h	AP: Virtual screen horizontal size is 128 addresses (REG[06h] bits 7-0, REG[07h] bits 7-0)
	P8 = 00h	
4	SCROLL	
	C = 44h	
	P1 = 00h	First screen block start address (REG[0Bh] bits 7-0, REG[0Ch] bits 7-0)
	P2 = 00h	Set to 0000h
	P3 = 40h	Display lines in first screen block = 64 (REG[0Dh] bits 7-0)
	P4 = 00h	Second screen block start address (REG[0Eh] bits 7-0, REG[0Fh] bits 7-0)
	P5 = 10h	Set to 1000h
	P6 = 40h	Display lines in second screen block = 64 (REG[10h] bits 7-0)
	P7 = 00h	Third screen block start address (REG[11h] bits 7-0, REG[12h] bits 7-0)
	P8 = 04h	Set to 0400h
	P9 = 00h	Fourth screen block start address (REG[13h] bits 7-0, REG[14h] bits 7-0)
	P10 = 30h	Set to 3000h
		
5	HDOT SCR	
	C = 5Ah	
	P1 = 00h	Set horizontal pixel shift to zero (REG[1Bh] bits 2-0)
6	OVLAY	
	C = 5Bh	
	P1 = 01h	MX 1, MX 0: Inverse video superposition (REG[18h] bits 1-0)
		DM 1: First screen block is text mode (REG[18h] bit 2)
		DM 2: Third screen block is text mode (REG[18h] bit 3)

Table 15-2 Indirect Addressing Initialization Procedure (Continued)

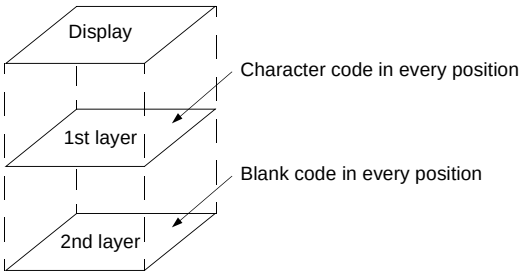
No.	Command	Operation
7	DISP ON/OFF	
	C = 58h	D: Display OFF (REG[09h] bit 0)
	P1 = 56h	FC1, FC0: Flash cursor at 2 Hz (REG[0Ah] bits 1-0)
	FP1, FP0:	First screen block ON (REG[0Ah] bits 3-2)
	FP3, FP2:	Second and fourth screen blocks ON (REG[0Ah] bits 5-4)
	FP5, FP4:	Third screen block ON (REG[0Ah] bits 7-6)
8	Clear data in first layer	Fill first screen layer memory with 20h (space character)
9	Clear data in second layer	Fill second screen layer memory with 00h (blank data) 
10	CSRW	
	C = 46h	
	P1 = 00h	Set cursor to start of first screen block (REG[1Ch] bits 7-0, REG[1Dh] bits 7-0)
	P2 = 00h	
11	CSR FORM	
	C = 5Dh	
	P1 = 04h	CRX: Horizontal cursor size = 5 pixels (REG[15h] bits 3-0)
	P2 = 86h	CRY: Vertical cursor size = 7 pixels (REG[16h] bits 3-0)
		CM: Block cursor (REG[16h] bit 7)
12	DISP ON/OFF	
	C = 59h	Display ON 
13	CSR DIR	
	C = 4Ch	Set cursor shift direction to right (REG[17h] bits 1-0)
14	MWRITE	
	C = 42h	
	P1 = 20h	‘ ’
	P2 = 45h	‘E’
	P3 = 50h	‘P’
	P4 = 53h	‘S’

Table 15-2 Indirect Addressing Initialization Procedure (Continued)

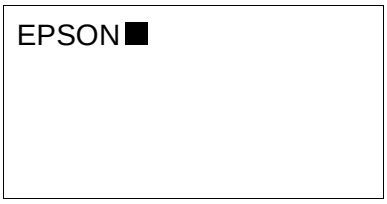
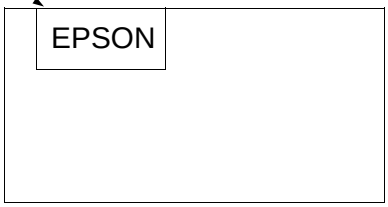
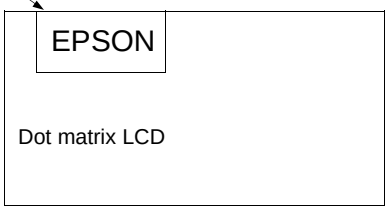
No.	Command	Operation
	P5 = 4Fh	'O'
	P6 = 4Eh	'N'
		
15	CSRW	
	C = 46h	
	P1 = 00h	Set cursor to start of second screen block (REG[1Ch] bits 7-0, REG[1Dh] bits 7-0)
	P2 = 10h	
16	CSR DIR	
	C = 4Fh	Set cursor shift direction to down (REG[17h] bits 1-0)
17	MWRITE	
	C = 42h	
	P1 = FFh	Fill in a square to the left of the 'E'
	↓	
	P9 = FFh	
		
18	CSRW	
	C = 46h	
	P1 = 01h	Set cursor address to 1001h (REG[1Ch] bits 7-0, REG[1Dh] bits 7-0)
	P2 = 10h	
19	MWRITE	
	C = 42h	
	P1 = FFh	Fill in the second screen block in the second column of line 1
	↓	
	P9 = FFh	
20	CSRW	Repeat operations 18 and 19 to fill in the background under 'EPSON' (REG[1Ch] bits 7-0, REG[1Dh] bits 7-0)

Table 15-2 Indirect Addressing Initialization Procedure (Continued)

No.	Command	Operation
		Inverse display 
↓		
29	MWRITE	
30	CSRW	
	C = 46h	
	P1 = 00h	Set cursor to line three of the first screen block (REG[1Ch] bits 7-0, REG[1Dh] bits 7-0)
	P2 = 01h	
31	CSR DIR	
	C = 4Ch	Set cursor shift direction to right (REG[17h] bits 1-0)
32	MWRITE	
	C = 42h	
	P1 = 44h	‘D’
	P2 = 6Fh	‘o’
	P3 = 74h	‘t’
	P4 = 20h	‘ ’
	P5 = 4Dh	‘M’
	P6 = 61h	‘a’
	P7 = 74h	‘t’
	P8 = 72h	‘r’
	P9 = 69h	‘i’
	P10 = 78h	‘x’
	P11 = 20h	‘ ’
	P12 = 4Ch	‘L’
	P13 = 43h	‘C’
	P14 = 44h	‘D’
		Inverse display 

15.1.3 Display Mode Setting Example 1: Combining Text and Graphics

Conditions

- 320 × 200 pixels, single panel drive (1/200 duty cycle)
- First layer: text display
- Second layer: graphics display
- 8 × 8-pixel character font
- CGRAM not required

Display memory allocation

- First layer (text): 320 ÷ 8 = 40 characters per line, 200 ÷ 8 = 25 lines. Required memory size = 40 × 25 = 1000 bytes.
- Second layer (graphics): 320 ÷ 8 = 40 characters per line, 200 ÷ 1 = 200 lines. Required memory size = 40 × 200 = 8000 bytes.

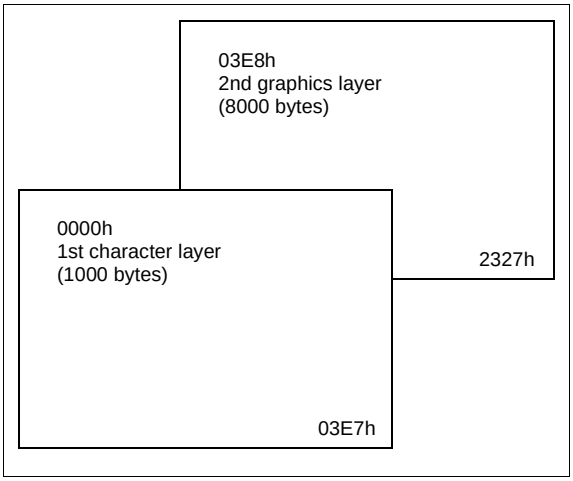


Figure 15-2 Character Over Graphics Layers

Register Setup Procedure

SYSTEM SET	TC/R calculation
C = 40h	
P1 = 30h	fOSC = 6 MHz (refer to Section 15.1.1, “SYSTEM SET Command and Parameters” on page 101)
P2 = 87h	fFR = 70 Hz (refer to Section 15.1.1, “SYSTEM SET Command and Parameters” on page 101)
P3 = 07h	
P4 = 27h	
P5 = 34h	[TC/R] = 52, so TC/R = 34h
P6 = C7h	
P7 = 28h	
P8 = 00h	
SCROLL	
C = 44h	
P1 = 00h	
P2 = 00h	
P3 = C8h	
P4 = E8h	
P5 = 03h	
P6 = C8h	
P7 = Xh	
P8 = Xh	
P9 = Xh	
P10 = Xh	
CSRFORM	
C = 5Dh	
P1 = 04h	
P2 = 86h	
HDOT SCR	
C = 5Ah	
P1 = 00h	
OVLAY	
C = 5Bh	
P1 = 00h	
DISP ON/OFF	
C = 59h	
P1 = 16h	

X = Don’t care

15.1.4 Display Mode Setting Example 2: Combining Graphics and Graphics

Conditions

- 320 × 200 pixels, single-panel drive (1/200 duty cycle)
- First layer: graphics display
- Second layer: graphics display

Display memory allocation

- First layer (graphics): 320 ÷ 8 = 40 characters per line, 200 ÷ 1 = 200 lines. Required memory size = 40 × 200 = 8000 bytes.
- Second layer (graphics): 320 ÷ 8 = 40 characters per line, 200 ÷ 1 = 200 lines. Required memory size = 8000 bytes.

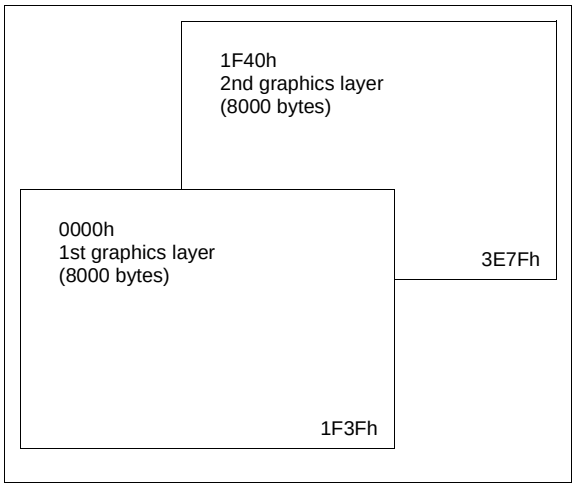


Figure 15-3 Two-Layer Graphics

Register setup procedure

SYSTEM SET	TC/R calculation
C = 40h	
P1 = 30h	f_{OSC} = 6 MHz (refer to Section 15.1.1, “SYSTEM SET Command and Parameters” on page 101)
P2 = 87h	f_{FR} = 70 Hz (refer to Section 15.1.1, “SYSTEM SET Command and Parameters” on page 101)
P3 = 07h	
P4 = 27h	
P5 = 34h	[TC/R] = 52, so TC/R = 34h
P6 = C7h	
P7 = 28h	
P8 = 00h	
SCROLL	
C = 44h	
P1 = 00h	
P2 = 00h	
P3 = C8h	
P4 = 40h	
P5 = 1Fh	
P6 = C8h	
P7 = Xh	
P8 = Xh	
P9 = Xh	
P10 = Xh	
CSRFORM	
C = 5Dh	
P1 = 07h	
P2 = 87h	
HDOT SCR	
C = 5Ah	
P1 = 00h	
OVLAY	
C = 5Bh	
P1 = 0Ch	
DISP ON/OFF	
C = 59h	
P1 = 16h	

X = Don’t care

15.1.5 Display Mode Setting Example 3: Combining Three Graphics Layers

Conditions

- 320 × 200 pixels, single-panel drive (1/200 duty cycle)
- First layer: graphics display
- Second layer: graphics display
- Third layer: graphics display

Display memory allocation

- All layers (graphics): 320 ÷ 8 = 40 characters per line, 200 ÷ 1 = 200 lines. Required memory size = 40 × 200 = 8000 bytes.

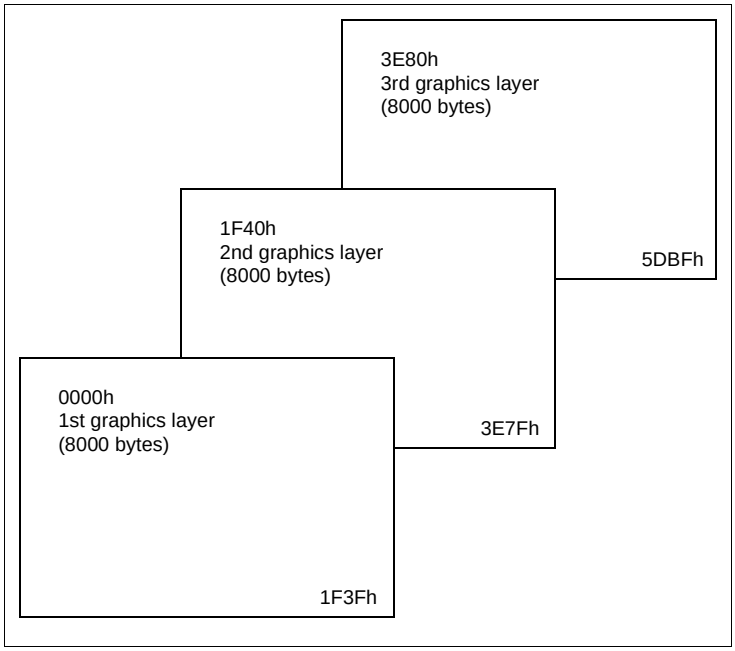


Figure 15-4 Three-Layer Graphics

Register setup procedure

SYSTEM SET	TC/R calculation
C = 40h	
P1 = 30h	f_{OSC} = 6 MHz (refer to Section 15.1.1, “SYSTEM SET Command and Parameters” on page 101)
P2 = 87h	f_{FR} = 70 Hz (refer to Section 15.1.1, “SYSTEM SET Command and Parameters” on page 101)
P3 = 07h	
P4 = 27h	
P5 = 34h	[TC/R] = 52, so TC/R = 34h
P6 = C7h	
P7 = 28h	
P8 = 00h	
SCROLL	
C = 44h	
P1 = 00h	
P2 = 00h	
P3 = C8h	
P4 = 40h	
P5 = 1Fh	
P6 = C8h	
P7 = 80h	
P8 = 3Eh	
P9 = Xh	
P10 = Xh	
CSR FORM	
C = 5Dh	
P1 = 07h	
P2 = 87h	
HDOT SCR	
C = 5Ah	
P1 = 00h	
OVLAY	
C = 5Bh	
P1 = 1Ch	
DISP ON/OFF	
C = 59h	
P1 = 16h	

X = Don’t care

15.2 System Overview

Section 3, “System Diagrams” on page 10 shows some typical S1D13700F01 implementations where the microprocessor issues instructions to the S1D13700F01, and the S1D13700F01 drives the LCD panel. Since the S1D13700F01 integrates all required LCD control circuits, minimal external components are required to construct a complete medium- resolution liquid crystal display solution.

15.3 Smooth Horizontal Scrolling

The S1D13700F01 supports smooth horizontal scrolling to the left as shown in Figure 15-5 “HDOT SCR Example,” on page 116. When scrolling left, the screen is effectively moving to the right over the larger virtual screen.

Instead of changing the screen block start address (SADx) and shifting the display by eight pixels, smooth scrolling is achieved by repeatedly changing the horizontal pixel scroll parameter of the HDOT SCR command (REG[1Bh] bits 2-0). When the display has been scrolled seven pixels, the horizontal pixel scroll parameter is reset to zero and screen block start address is incremented by one. Repeating this operation at a suitable rate gives the appearance of smooth scrolling.

Note
To scroll the display to the right, the procedure is reversed.

When the edge of the virtual screen is reached, the microprocessor must take appropriate steps to avoid corrupting the display. For example, scrolling must be stopped or the display must be modified.

Note
The HDOT SCR command cannot be used to scroll individual layers.

Note
When in 2 bpp or 4 bpp mode, smooth horizontal scrolling in pixel units is not supported.

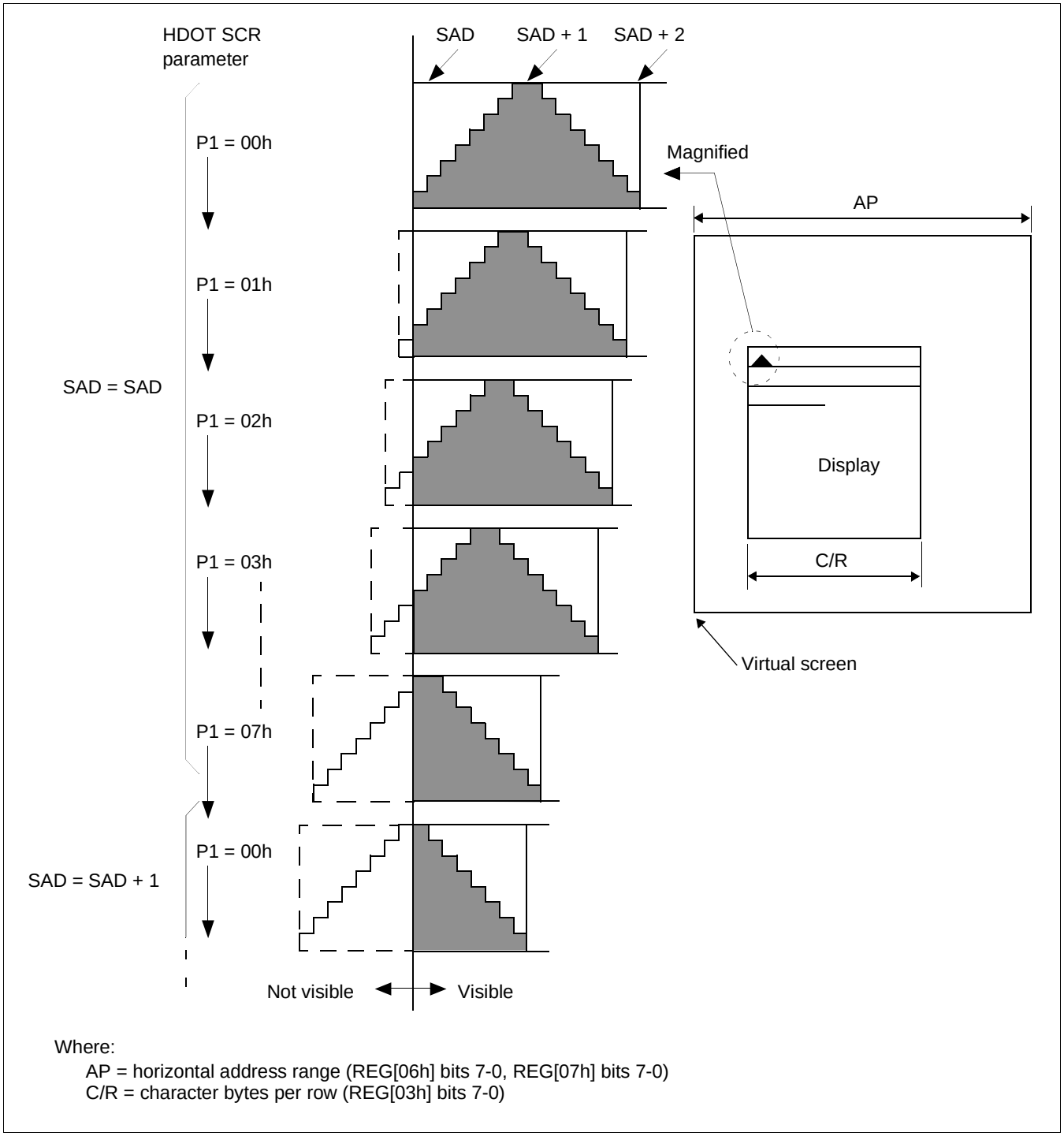


Figure 15-5 HDOT SCR Example

Note

The response time of LCD panels changes considerably at low temperatures. Smooth scrolling under these conditions may make the display difficult to read.

15.4 Layered Display Attributes

S1D13700F01 incorporates a number of functions for enhancing displays using monochrome LCD panels. It allows the display of inverse characters, half-intensity menu pads and flashing of selected screen areas. These functions are controlled by REG[18h] Overlay Register and REG[0Ah] Display Attribute Register.

Attribute	MX1	MX0	Combined Layer Display	1st Layer Display	2nd Layer Display
Reverse	0	1	IV EPSON	IV EPSON	
Half-tone	0	0	ME Yes, No	ME Yes, No	
Local flashing	0 0	0 1	BL Error	BL	Error
Ruled line	0 0	0 1	RL LINE LINE	RL LINE LINE	

Figure 15-6 Layer Synthesis

These effects can be achieved in different ways, depending on the display configuration. The following sections describe these functions.

Note
Not all functions can be used in one layer at the same time.

15.4.1 Inverse Display

For inverse display where the first layer is text and the second layer is graphics.

1. CSRW, CSRDIR, MWRITE

   Write to the graphics screen at the area to be inverted.

2. OVLAY: MX0 = 1, MX1 = 0 (REG[18h] bits 1-0)

   Set the layer compensation method of the two layers to Exclusive-OR.

3. DISP ON/OFF: FP0 = 1, FP1 = 0, FP2 = 1, FP3 = 0.

   Turn on layers 1 and 2 with no flashing.

15.4.2 Half-Tone Display

The FP parameter (display attributes) can be used to generate a half-intensity display by flashing the display at 17Hz. Note that this mode may cause flicker problems with certain LCD panels.

Menu Pad Display

Turn flashing off for the first layer, on at 17 Hz for the second layer, and combine the screens using the OR function.

1. REG[18h] Overlay Register = 00h
2. REG[0Ah] Display Attribute Register = 34h

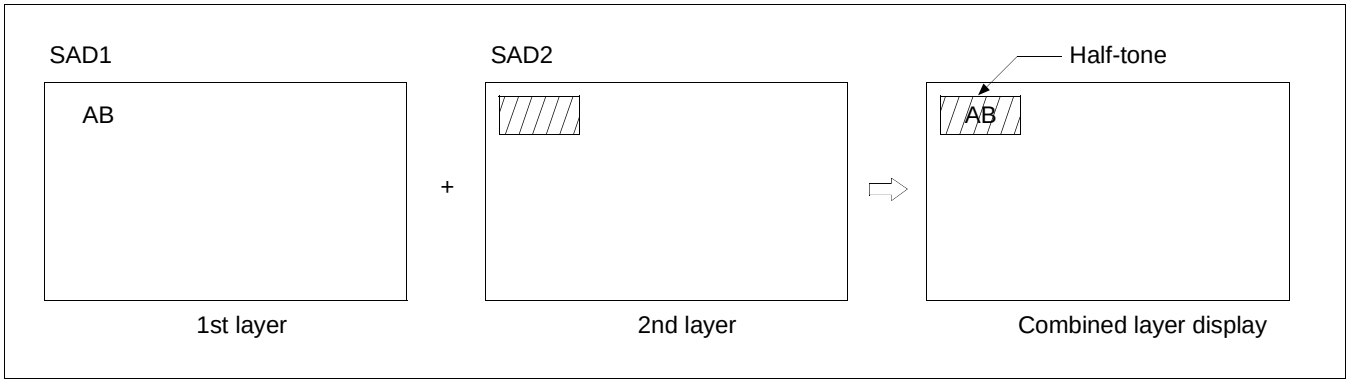


Figure 15-7 Half-Tone Character And Graphics

Graph Display

To display two overlaid graphs on the screen, configure the display in the same manner as for menu pad display and put one graph on each screen layer. The difference in contrast between the half and full intensity displays make it easy to distinguish between the two graphs and create an attractive display.

1. REG[18h] Overlay Register = 00h
2. REG[0Ah] Display Attribute Register = 34h

15.4.3 Flash Attribute

Small Area

To flash selected characters, the MPU can alternately write the characters as character codes and blank characters at intervals of 0.5 to 1.0 seconds.

Large Area

Divide both layer 1 and layer 2 into two screen blocks each, layer 2 being divided into the area to be flashed and the remainder of the screen. Flash the layer 2 screen block at 2 Hz for the area to be flashed and combine the layers using the OR function.

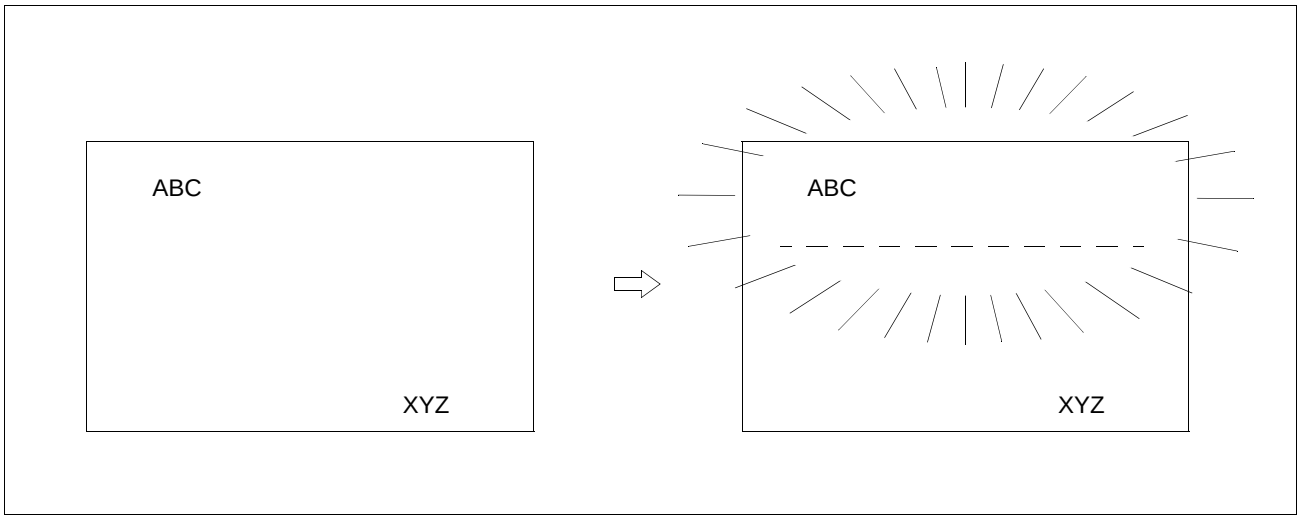


Figure 15-8 Flash Attribute for a Large Area

15.5 16 × 16-Dot Graphic Display

15.5.1 Command Usage

To display 16 × 16 pixel characters, use the following procedure.

1. Set the cursor address, REG[1Ch] - REG[1Dh]
2. Set the cursor shift direction, REG[17h] bits 1-0
3. Write to the display memory

15.5.2 Kanji Character Display

To write large characters, use the following procedure. For further information, see the flowchart in Figure 15-9 “Graphics Address Indexing,” on page 121.

1. Reads the character data from the CGRAM
2. Set the display address
3. Writes to the display memory

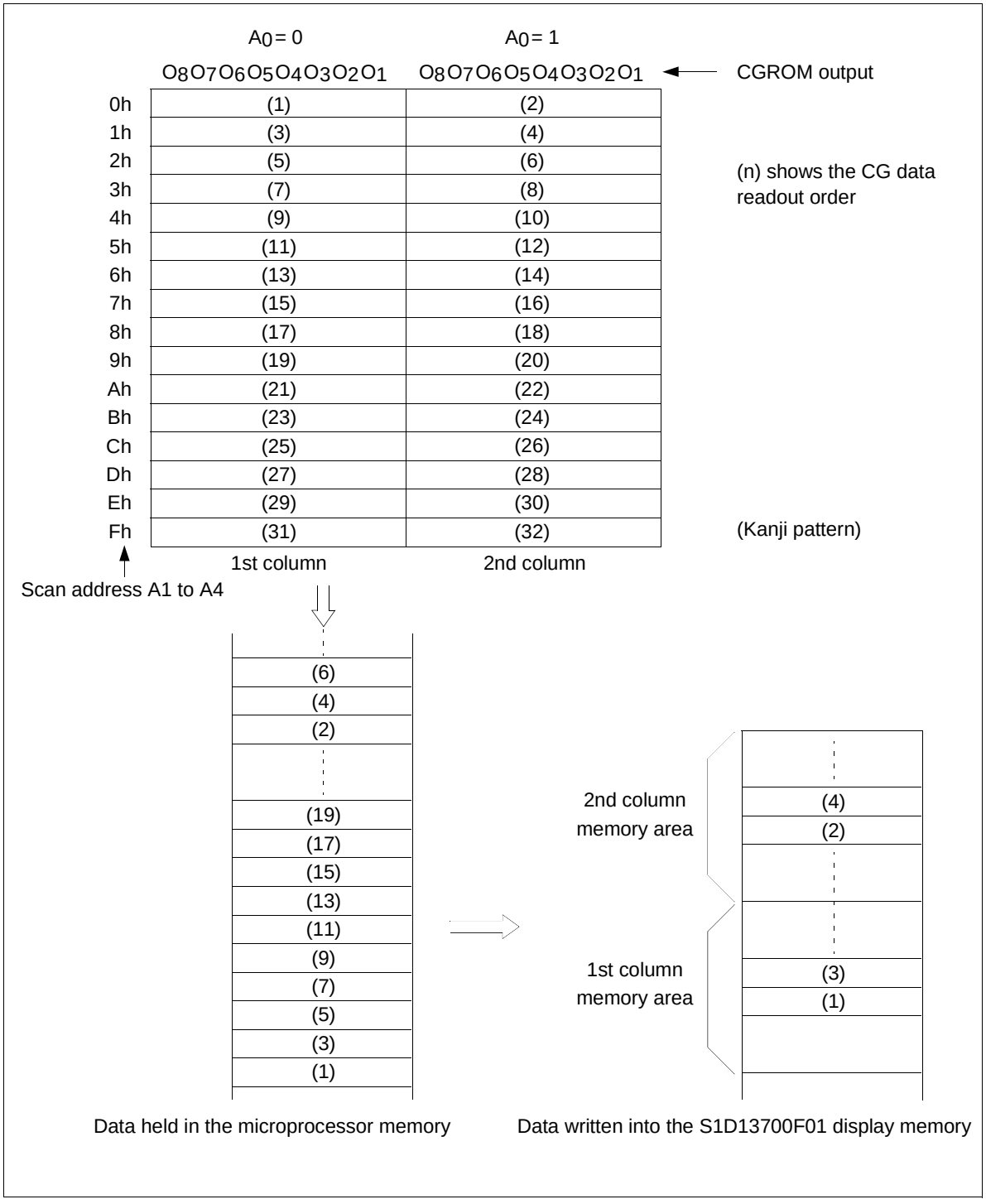


Figure 15-9 Graphics Address Indexing

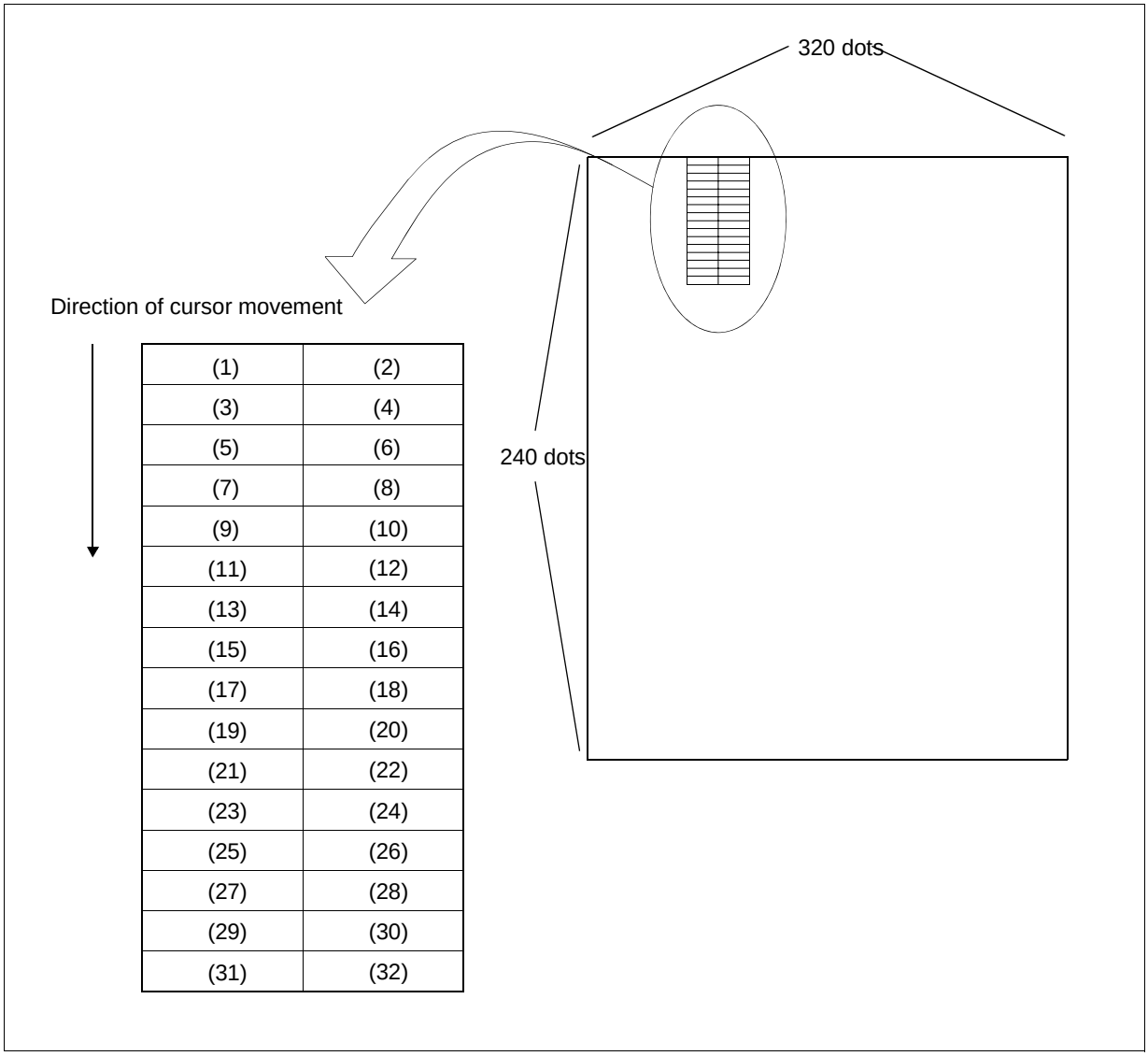
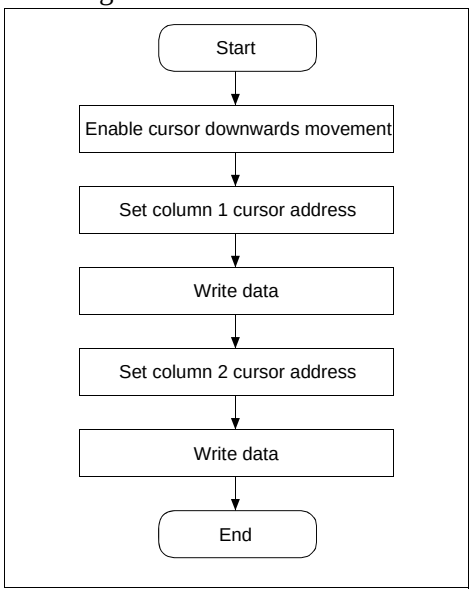


Figure 15-10 Graphics Bit Map

Using an external character generator RAM an 8×16 pixel font can be used, which allows a 16×16 pixel character to be displayed in two segments. The CGRAM data format is described in Figure 13 “Character Generator,” on page 95. This allows the display of up to 128, 16×16 pixel characters. If CGRAM is also used, 96 fixed characters and 32 bank-switchable characters are also be supported.

For Direct Addressing Mode



For Indirect Addressing Mode

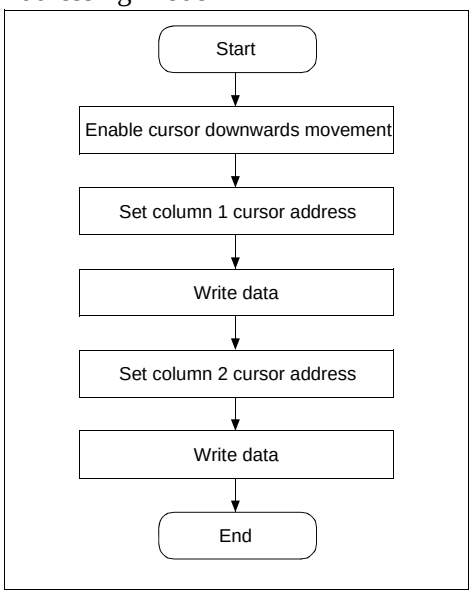


Figure 15-11 16 × 16-Dot Display Flowchart

16 Internal Character Generator Font

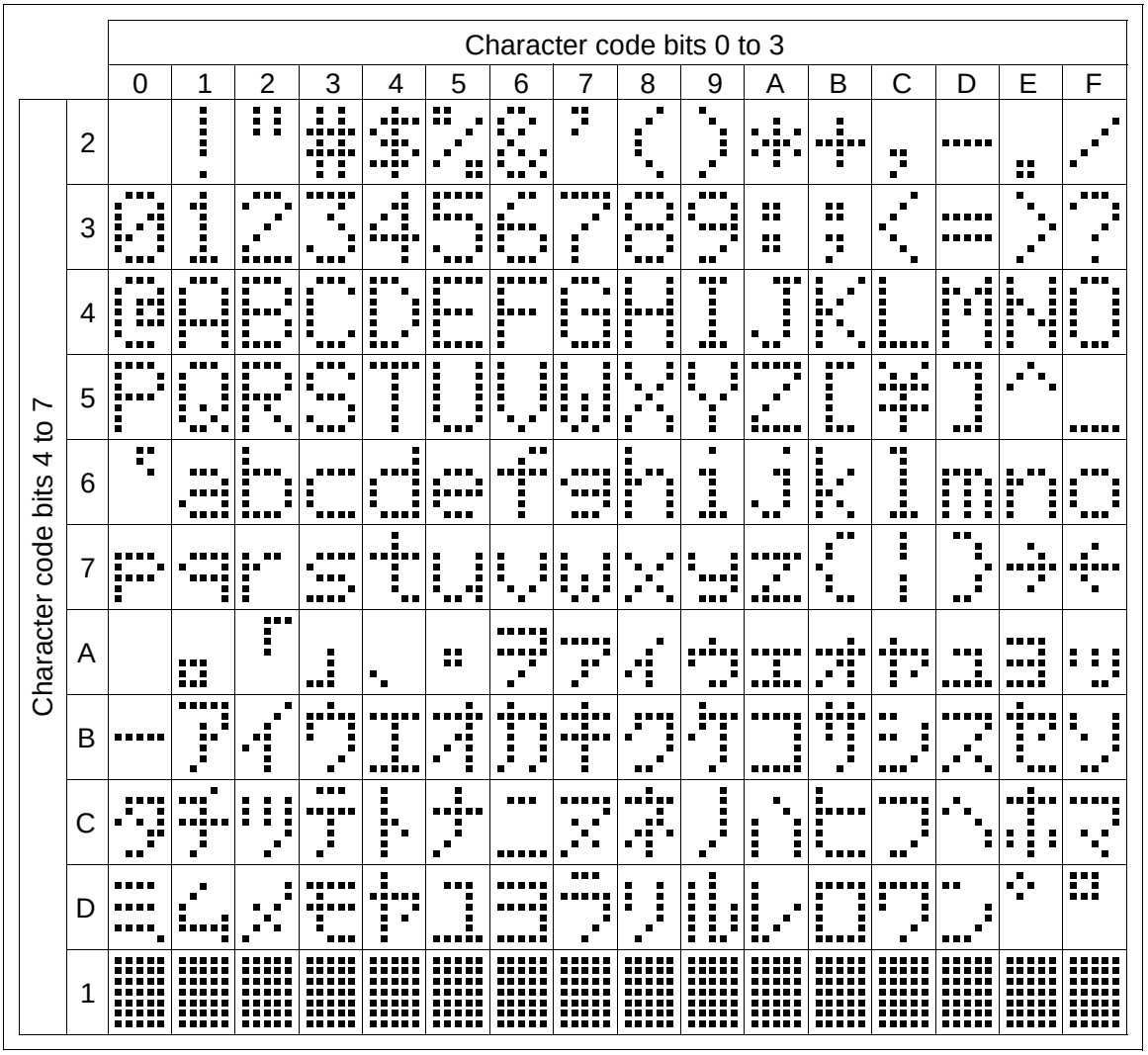


Figure 16-1 On-Chip Character Set

Note

The shaded positions indicate characters that have the whole 6×8 bitmap blackened.

17 Power Save Mode

The S1D13700F01 supports a power save mode that places it into a power efficient state. Power save mode is controlled by the Power Save Mode Enable bit, REG[08h] bit 0. The S1D13700F01 enters power save mode at least one blank frame after the enable bit is set.

When power save mode is enabled, blank data is sent to the X-drivers, and the Y-drivers have their bias supplies turned off by the YDIS signal. Using the YDIS signal to disable the Y-drivers guards against any spurious displays. The internal registers of the S1D13700F01 maintain their values during the power save state and the display memory control pins maintain their logic levels to ensure that the display memory is not corrupted.

The S1D13700F01 is removed from power save mode by writing a 0 the Power Save Mode Enable bit, REG[08h] bit 0. However, after disabling power save mode, one dummy write to any register must be performed for direct addressing mode, and at least two dummy writes must be performed for indirect addressing mode.

For indirect addressing mode, the POWER SAVE command has no parameter bytes. For indirect addressing mode, the SYSTEM SET command exits power save mode.

1. The YDIS signal goes LOW between one and two frames after the power save command is received. Since YDIS forces all display driver outputs to go to the deselected output voltage, YDIS can be used as a power down signal for the LCD unit. This can be done by having YDIS turn off the relatively high power LCD drive supplies at the same time as it blanks the display.

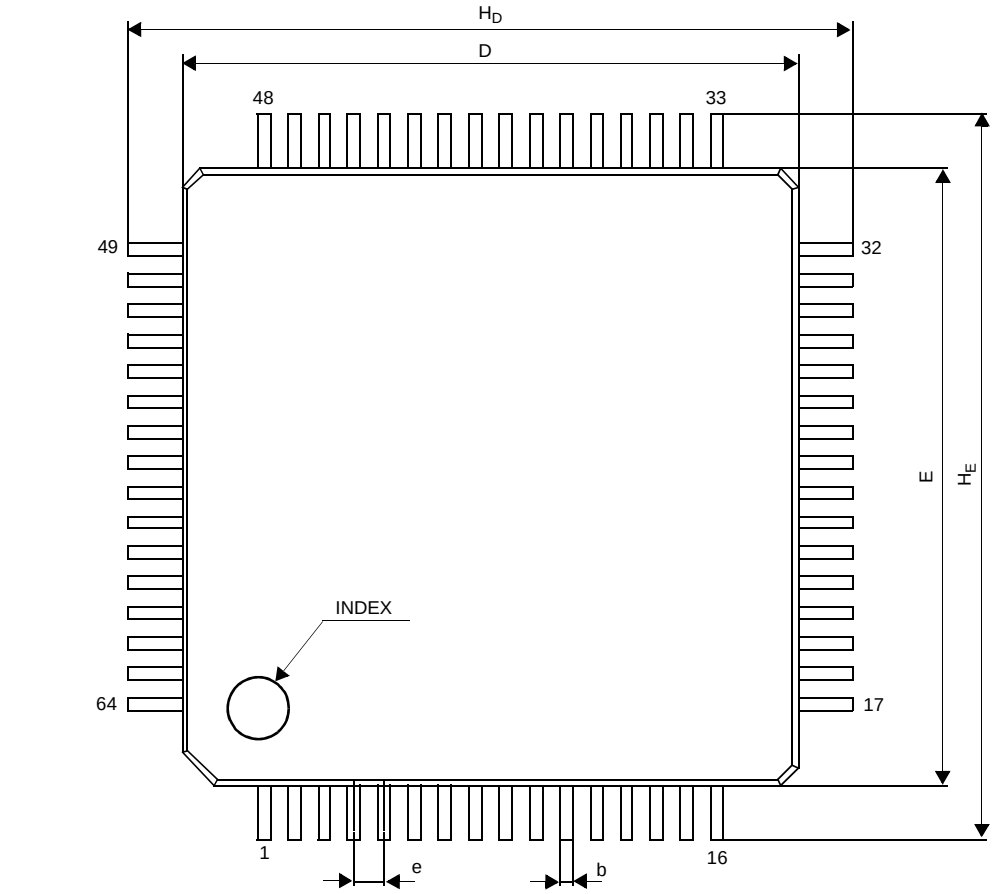
2. Since all internal clocks in the S1D13700F01 are halted while power save mode is enabled, a DC voltage is applied to the LCD panel if the LCD drive supplies remain on. If reliability is a prime consideration, turn off the LCD drive supplies before issuing the power save command.

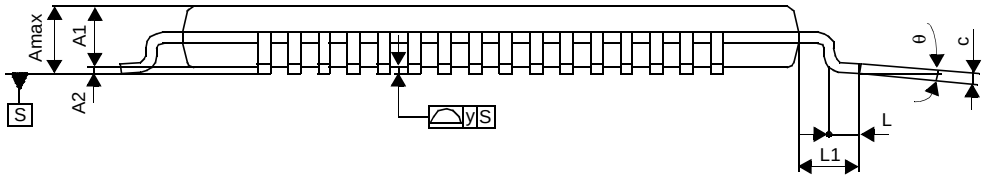
3. The bus lines become high impedance when power save mode is enabled. If the bus is required to be a known state, pull-up or pull-down resistors can be used.

Table 17-1 State of LCD Pins During Power Save Mode

LCD Pin	State During Display Off	State During Power Save Mode
YDIS	Low	Low
FPFRAME	Low	Low
YSCL	High	High
MOD	Low	Low
FPLINE	Low	Low
XECL	Low	Low
FPSHIFT	Low	Low
FPDAT[3:0]	Low	Low
WAIT#	Hi-Z	Hi-Z
DB[7:0]	Hi-Z	Hi-Z
XCD1	High	High

18 Mechanical Data





Symbol	Dimension in Millimeters		
	Min	Nom	Max
E	-	10.0	-
D	-	10.0	-
Amax	-	-	1.2
A1	-	0.1	-
A2	-	1.0	-
e	-	0.5	-
b	0.17	-	0.27
c	0.09	-	0.2
θ	0°	-	10°
L	0.3	-	0.75
L1	-	1.0	-
H_E	-	12.0	-
H_D	-	12.0	-
y	-	-	0.08

All dimensions in mm

Figure 18-1 Mechanical Drawing TQFP13 - 64 pin

19 References

The following documents contain additional information related to the S1D13700F01. Document numbers are listed in parenthesis after the document name. All documents can be found at the Epson Research and Development Website at **www.erd.epson.com**.

- S1D13700 Product Brief (X42A-A-002-xx)

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Change Record

X42A-A-001-04 Revision 4.03

- section 5.4, fixed typos of pin names in Host Interface Pin Mapping table, “AB” should be “A” and “DB” should be “D”
- section 7.3, fixed typos of pin names in Host Interface Timing section, “AB” should be “A” and “DB” should be “D”
- section 7.2, updated the reset timing section to clarify the “Oscillator stable delay” and “Reset pulse duration”
- section 7.3.6, added new section for Display Memory Access timing
- section 12.2.3, added reference to new section for Display Memory Access timing and added note about text mode

X42A-A-001-04 Revision 4.02

- section 5.4, updated the Host Interface Pin Mapping Table, AS# for the M6800 Indirect mode is changed to “Connected to HIOVDD” instead of “Connected to VSS”
- section 7.3.5, updated the M6800 Family Bus Indirect Interface Timing diagram to removed AS# and t13, t14, also removed t13, t14 from the timing table
- section 9.2.1, in system clock section, changed the 2 occurrences of “internal crystal” with “internal oscillator (with external crystal)”
- section 10.3.1, in the System Control Registers section, changed “'The SYSTEM SET command is used to initialize the S1D13700F01 and the display **when indirect addressing is used.**” to “The SYSTEM SET command is used to configure the S1D13700F01 for the display used and to exit power save mode **when indirect addressing is used**.”
- section 10.3.1, in the Power Save Registers section, changed “'standby mode” to “power save mode” and added the following note “The SYSTEM SET command is used to exit power save mode, when indirect addressing is used. For further information on the SYSTEM SET command, see section 11.1.1, “SYSTEM SET” on page 71.”
- REG[08h], reserved the information in the first note about disabling power save mode for indirect interface and added the following information to the note as engineering text “In indirect mode, SYSTEM SET command is used to exit power save mode. After writing parameter P1 of SYSTEM SET command, 13700 will exit power save mode and REG[08h]bit0=0. To complete SYSTEM SET command, parameters P2-P8 must also be written, so the requirement for at least 2 writes to any register is automatically satisfied at the end of SYSTEM SET command.”
- section 11.1.1, in the SYSTEM SET section, added the following note “If the S1D13700F01 is in power save mode (at power up or after a POWER SAVE command), the SYSTEM SET command will exit power save mode. After writing the SYSTEM SET command and its 8 parameters, the S1D13700F01 will be in normal operation.”

- section 15.1.1, replaced SYSTEM SET Command and Parameters section
- section 18, updated mechanical drawing sizes

X42A-A-001-04 Revision 4.01

- section 7.3.1, updated typos in timing table notes 4 and 5
- section 7.3.3, updated typos in timing table notes 4 and 5
- section 7.3.5, updated typos in timing table notes 4 and 5
- section 10.3, updated the register headings to include default values

X42A-A-001-04 Revision 4.0

- released as revision 4.0

X42A-A-001-03 Revision 3.01

- section 7.3.3, fixed note 6 in the table, should reference t17 parameter instead of t20
- section 7.3.4, fixed note 4 in the table, should reference t10 parameter instead of t13
- section 7.3.4, fixed note 5 in the table, should reference t12 parameter instead of t15

X42A-A-001-03 Revision 3.0

- released as revision 3.0

X42A-A-001-02 Revision 2.01

- section 2.8, removed Pb-used package
- section 5.1, changed pinout diagram to show “D1370001A1” on package instead of “S1D13700F01”

X42A-A-001-02 Revision 2.0

- released as revision 2.0

X42A-A-001-01 Revision 1.01

- section 10.3.4, added note about gray scale only available for layer 1
- section 11.1.2, changed bit 3 value from 01 to 0
- section 15.1.1, updated formulas for 1, 2, 4 bpp in system set section
- table 15-1, changed TC/R value for 256x64 from 24h to 2Eh
- table 15-1, changed TC/R value for 256x128 from 16h to 24h

X42A-A-001-01 Revision 1.0

- released as revision 1.0

X42A-A-001-00 Revision 0.01

- started from S1D13700F00 Hardware Specification (X42A-A-001-xx)
- section 7.3, removed parameters t12, t13, t14 from the timing diagrams/tables with WAIT#/DTACK#

- section 7.3.3, changed references in the timing table from “WAIT#” to “DTACK#”
- section 7.3.5, removed note about CLK input under the M6800 diagram
- table 9-1, for parameter Rd, typical is 100ohm not 100Kohm
- REG[00h] bit 0, added note about 1bpp only when CGRAM is used
- REG[0Bh] - REG[0Ch], added note about programming the LSB before the MSB
- REG[0Eh] - REG[0Fh], added note about programming the LSB before the MSB
- REG[11h] - REG[12h], added note about programming the LSB before the MSB
- REG[13h] - REG[14h], added note about programming the LSB before the MSB
- REG[20h], added information about 1bpp only when CGRAM is used
- section 15.1.5, removed note about line noise during three layer graphics mode
- section 13.1.3, added note about 1bpp only when CGRAM is used
- section 13.3, added note about 1bpp only when CGRAM is used
- section 15.1.1, updated TC/R’ formulas for 1 Bpp and 2 Bpp
- section 19, added reference to the Product Brief