DATA SHEET

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SPLC780D1

16COM/40SEG Controller/Driver

Preliminary

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Version 0.1

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16COM / 40SEG CONTROLLER / DRIVER

1. GENERAL DESCRIPTION

The SPLC780D1, a dot-matrix LCD controller and driver from ORISE, is a unique design for displaying alpha-numeric, Japanese-Kana characters and symbols. The SPLC780D1 provides two types of interfaces to MPU: 4-bit and 8-bit interfaces. The transferring speed of 8-bit is twice faster than 4-bit. A single SPLC780D1 is able to display up to two 8-character lines. By cascading with SPLC100 or SPLC063, the display capability can be extended. The CMOS technology ensures the power saves in the most efficient way and the performance keeps in the highest rank.

2. FEATURES

- Character generator ROM: 10880 bits
  - Character font 5 x 8 dots: 192 characters
  - Character font 5 x 10 dots: 64 characters
- Character generator RAM: 512 bits
  - Character font 5 x 8 dots: 8 characters
  - Character font 5 x 10 dots: 4 characters
- 4-bit or 8-bit MPU interfaces
- Direct driver for LCD: 16 COMs x 40 SEGs
- Duty factor (selected by program):
  - 1/8 duty: 1 line of 5 x 8 dots
  - 1/11 duty: 1 line of 5 x 10 dots
  - 1/16 duty: 2 lines of 5 x 8 dots / line
- Built-in power on automatic reset circuit
- Built-in oscillator circuit (with external resistor)
- Support external clock operation
- Low Power Consumption
- Package form: 80 QFP or bare chip available

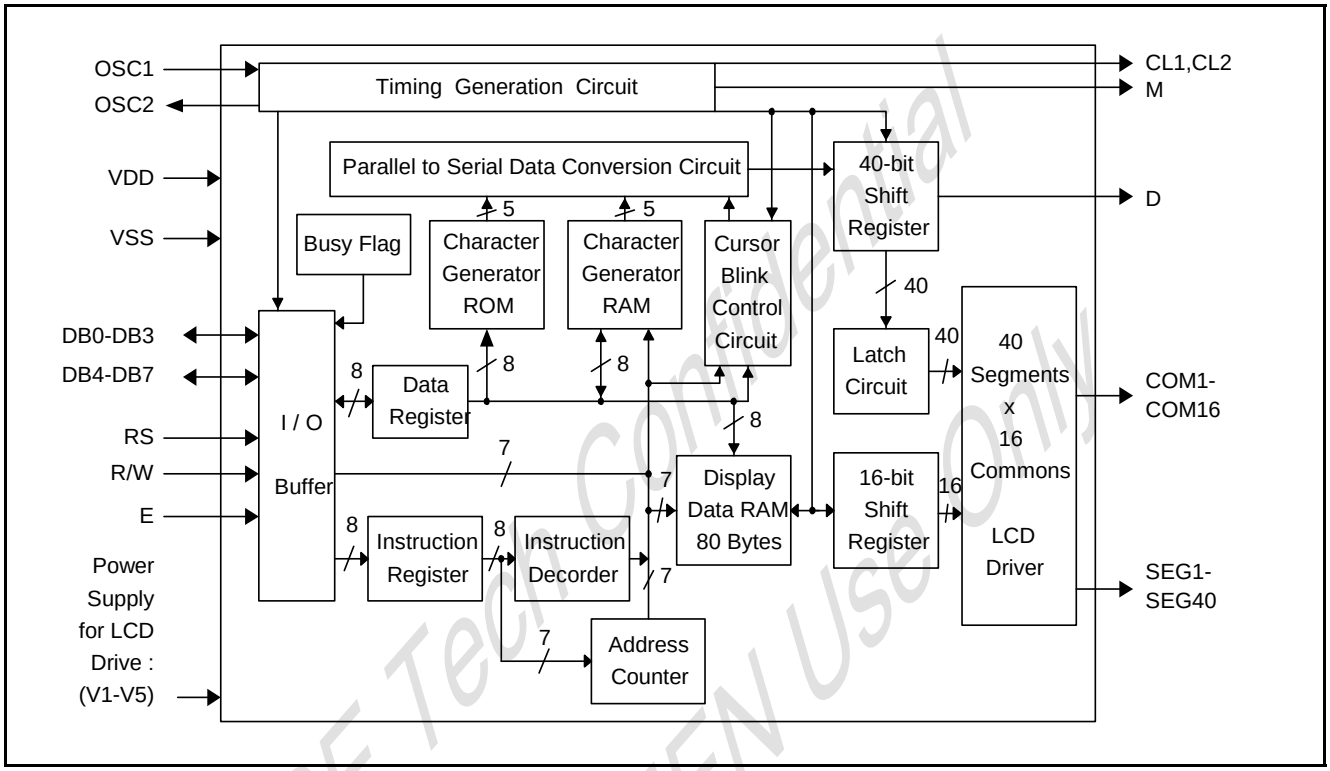
3. ORDERING INFOMATION

Product Number	Package Type
SPLC780D1-NnnV-C	Chip form
SPLC780D1-NnnV-HQ051	Green Package form - QFP 80L

Note1: Code number is assigned for customer.
Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

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4. BLOCK DIAGRAM



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5. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	Type	Description
VDD	33	I	Power input
VSS	23	I	Ground
OSC1 OSC2	24 25	-	Both OSC1 and OSC2 are connected to resistor for internal oscillator circuit. For external clock operation, the clock is input to OSC1.
V1 - V5	26 - 30	I	Supply voltage for LCD driving.
E	38	I	A start signal for reading or writing data.
R/W	37	I	A signal for selecting read or write actions. 1: Read, 0: Write.
RS	36	I	A signal for selecting registers. 1: Data Register (for read and write) 0: Instruction Register (for write), Busy flag - Address Counter (for read).
DB0 - DB3	39 - 42	I/O	Low 4-bit data
DB4 - DB7	43 - 46	I/O	High 4-bit data
CL1	31	O	Clock to latch serial data D.
CL2	32	O	Clock to shift serial data D.
M	34	O	Switch signal to convert LCD waveform to AC.
D	35	O	Sends character pattern data corresponding to each common signal serially. 1: Selection, 0: Non-selection.
SEG1 - SEG22 SEG23 - SEG40	22 - 1 80 - 63	O	Segment signals for LCD.
COM1 - COM16	47 - 62	O	Common signals for LCD.

6. COMPARISON OF SPLC780D AND SPLC780D1

	SPLC780D	SPLC780D1	Memo
Chip size	2860u*2450u	2860u*2450u	
PAD Size	90u * 90u	90u * 90u	Passivation Opening Window
Min. PAD Pitch	110u	110u	
LCD Voltage(V_{LCD})	3V ~ 9V	3V ~ 8V	
Absolute Maximum Rating	12v	10v	

Note: SPLC780D1 and SPLC780D have the same chip size and pad location.

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7. FUNCTIONAL DESCRIPTIONS

7.1. Oscillator

SPLC780D1 oscillator supports not only the internal oscillator operation, but also the external clock operation.

7.2. Control and Display Instructions

Control and display instructions are described in details as follows:

7.2.1. Clear display

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	0	1

It clears the entire display and sets Display Data RAM Address 0 in Address Counter.

7.2.2. Return home

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	1	X

X: Do not care (0 or 1)

It sets Display Data RAM Address 0 in Address Counter and the display returns to its original position. The cursor or blink goes to the most-left side of the display (to the 1st line if 2 lines are displayed). The contents of the Display Data RAM do not change.

7.2.3. Entry mode set

During writing and reading data, it defines cursor moving direction and shifts the display.

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	1	I / D	S

I / D = 1: Increment, I / D = 0: Decrement.

S = 1: The display shift, S = 0: The display does not shift.

S = 1	I / D = 1	It shifts the display to the left
S = 1	I / D = 0	It shifts the display to the right

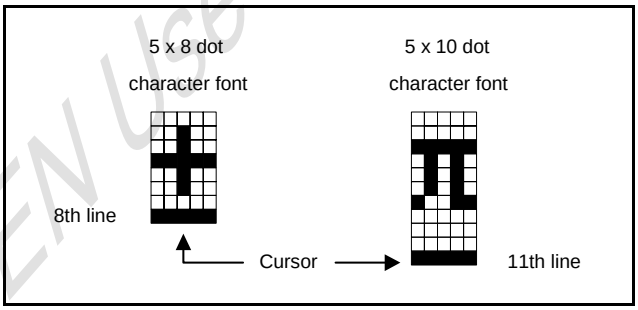
7.2.4. Display ON/OFF control

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	1	D	C	B

D = 1: Display on, D = 0: Display off

C = 1: Cursor on, C = 0: Cursor off

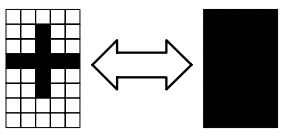
B = 1: Blinks on, B= 0: Blinks off



7.2.5. Cursor or display shift

Without changing DD RAM data, it moves cursor and shifts display.

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	1	S/C	R/L	X	X



Blink display alternately

S/C	R/L	Description	Address Counter
0	0	Shift cursor to the left	AC = AC - 1
0	1	Shift cursor to the right	AC = AC + 1
1	0	Shift display to the left. Cursor follows the display shift	AC = AC
1	1	Shift display to the right. Cursor follows the display shift	AC = AC

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7.2.6. Function set

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	1	DL	N	F	X	X

X: Do not care (0 or 1)

DL: It sets interface data length.

DL = 1: Data transferred with 8-bit length (DB7 - 0).

DL = 0: Data transferred with 4-bit length (DB7 - 4).

It requires two times to accomplish data transferring.

N: It sets the number of the display line.

N = 0: One-line display.

N = 1: Two-line display.

F: It sets the character font.

F = 0: 5 x 8 dots character font.

F = 1: 5 x 10 dots character font.

N	F	No. of Display Lines	Character Font	Duty Factor
0	0	1	5 x 8 dots	1 / 8
0	1	1	5 x 10 dots	1 / 11
1	X	2	5 x 8 dots	1 / 16

It cannot display two lines with 5 x 10 dots character font.

7.2.7. Set character generator RAM address

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	1	a	a	a	a	a	a

It sets Character Generator RAM Address $(aaaaaa)_2$ to the Address Counter.

Character Generator RAM data can be read or written after this setting.

7.2.8. Set display data RAM address

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	1	a	a	a	a	a	a	a

It sets Display Data RAM Address $(aaaaaaa)_2$ to the Address Counter.

Display data RAM can be read or written after this setting.

In one-line display (N = 0),

$(aaaaaaa)_{2:}$ $(00)_{16}$ - $(4F)_{16.}$

In two-line display (N = 1),

$(aaaaaaa)_{2:}$ $(00)_{16}$ - $(27)_{16}$ for the first line,

$(aaaaaaa)_{2:}$ $(40)_{16}$ - $(67)_{16}$ for the second line.

7.2.9. Read busy flag and address

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	BF	a	a	a	a	a	a	a

When BF = 1, it indicates the system is busy now and it will not accept any instruction until not busy (BF = 0). At the same time, the content of Address Counter $(aaaaaaa)_2$ is read.

7.2.10. Write data to character generator RAM or display data RAM

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	0	d	d	d	d	d	d	d	d

It writes data $(dddddddd)_2$ to character generator RAM or display data RAM.

7.2.11. Read data from character generator RAM or display data RAM

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	1	d	d	d	d	d	d	d	d

It reads data $(dddddddd)_2$ from character generator RAM or display data RAM.

To read data correctly, do the following:

1). The address of the Character Generator RAM or Display Data RAM or shift the cursor instruction.

2). The " Read " instruction.

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7.3. Instruction Table

Instruction	Instruction Code										Description	Execution time (Temp = 25℃)		
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		Fosc= 190KHz	Fosc= 270KHz	Fosc= 350KHz
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM and set DDRAM address to "00H" from AC	2.16ms	1.52ms	1.18ms
Return Home	0	0	0	0	0	0	0	0	1	-	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	2.16ms	1.52ms	1.18ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Assign cursor moving direction and enable the shift of entire display	53μs	38μs	29μs
Display ON/ OFF Control	0	0	0	0	0	0	1	D	C	B	Set display (D), cursor(C), and blinking of cursor(B) on/off control bit.	53μs	38μs	29μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	-	-	Set cursor moving and display shift control bit, and the direction, without changing of DDRAM data.	53μs	38μs	29μs
Function Set	0	0	0	0	1	DL	N	F	-	-	Set interface data length (DL: 8-bit/4-bit), numbers of display line (N: 2-line/1-line) and, display font type (F:5x10 dots/5x8 dots)	53μs	38μs	29μs
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	53μs	38μs	29μs
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter	53μs	38μs	29μs
Read Busy Flag and Address Counter	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.			
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	53μs	38μs	29μs
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM).	53μs	38μs	29μs

Note1: "--": don't care

Note2: In the operation condition under -20℃ ~ 75℃, the maximum execution time for majority of instruction sets is 100us, except two instructions, "Clear Display" and "Return Home", in which maximum execution time can take up to 4.1ms.

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7.4. 8-Bit Operation and 8-Digit 1-Line Display (Using Internal Reset)

No.	Instruction	Display	Operation
1	Power on. (SPLC780D1 starts initializing)		Power on reset. No display.
2	Function set RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 0 0 X X		Set to 8-bit operation and select 1-line display line and character font.
3	Display on / off control 0 0 0 0 0 0 1 1 1 0	_	Display on. Cursor appear.
4	Entry mode set 0 0 0 0 0 0 0 1 1 0	_	Increase address by one. It will shift the cursor to the right when writing to the DD RAM/CG RAM. Now the display has no shift.
5	Write data to CG RAM / DD RAM 1 0 0 1 0 1 0 1 1 1	W_	Write " W ". The cursor is incremented by one and shifted to the right.
6	Write data to CG RAM / DD RAM 1 0 0 1 0 0 0 1 0 1	WE_	Write " E ". The cursor is incremented by one and shifted to the right.
7	:	:	
8	Write data to CG RAM / DD RAM 1 0 0 1 0 0 0 1 0 1	WELCOME_	Write " E ". The cursor is incremented by one and shifted to the right.
9	Entry mode set 0 0 0 0 0 0 0 1 1 1	WELCOME_	Set mode for display shift when writing
10	Write data to CG RAM / DD RAM 1 0 0 0 1 0 0 0 0 0	ELCOME _	Write " "(space). The cursor is incremented by one and shifted to the right.
11	Write data to CG RAM / DD RAM 1 0 0 1 0 0 0 0 1 1	LCOME C_	Write " C ". The cursor is incremented by one and shifted to the right.
12	:	:	
13	Write data to CG RAM / DD RAM 1 0 0 1 0 1 1 0 0 1	COMPAMY_	Write " Y ". The cursor is incremented by one and shifted to the right.
14	Cursor or display shift 0 0 0 0 0 1 0 0 X X	COMPAMY_	Only shift the cursor's position to the left (Y).
15	Cursor or display shift 0 0 0 0 0 1 0 0 X X	COMPAMY_	Only shift the cursor's position to the left (M).
16	Write data to CG RAM / DD RAM 1 0 0 1 0 0 1 1 1 0	OMPANY_	Write " N ". The display moves to the left.
17	Cursor or display shift 0 0 0 0 0 1 1 1 X X	COMPAMY_	Shift the display and the cursor's position to the right.
18	Cursor or display shift 0 0 0 0 0 1 0 1 X X	OMPANY_	Shift the display and the cursor's position to the right.
19	Write data to CG RAM / DD RAM 1 0 0 1 0 0 0 0 0 0	COMPAMY_	Write " " (space). The cursor is incremented by one and shifted to the right.
20	:	:	:
21	Return home 0 0 0 0 0 0 0 0 1 0	WELCOME_	Both the display and the cursor return to the original position (address 0).

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7.5. 4-Bit Operation and 8-Digit 1-Line Display (Using Internal Reset)

No.	Instruction	Display	Operation
1	Power on. (SPLC780D1 starts initializing)		Power on reset. No display.
2	Function set RS R/W DB7 DB6 DB5 DB4 0 0 0 0 1 0		Set to 4-bit operation.
3	0 0 0 0 1 0 0 0 0 0 X X		Set to 4-bit operation and select 1-line display line and character font.
4	0 0 0 0 0 0 0 0 1 1 1 0	_	Display on. Cursor appears.
5	0 0 0 0 0 0 0 0 0 1 1 0	_	Increase address by one. It will shift the cursor to the right when writing to the DD RAM / CG RAM. Now the display has no shift.
6	1 0 0 1 0 1 1 0 0 1 1 1	W_	Write " W ". The cursor is incremented by one and shifted to the right.

7.6. 8-Bit Operation and 8-Digit 2-Line Display (Using Internal Reset)

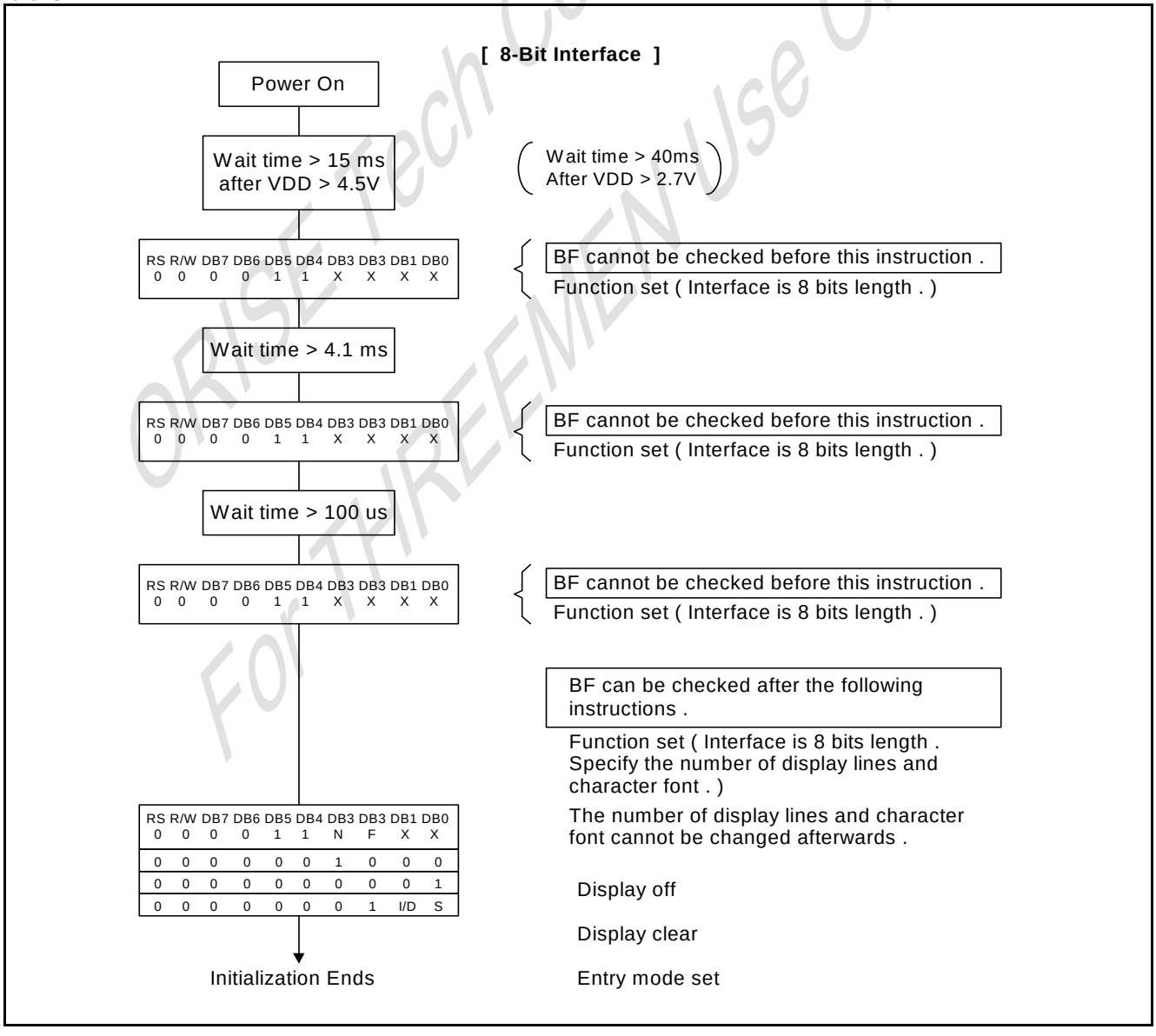
No.	Instruction	Display	Operation
1	Power on. (SPLC780D1 starts initializing)		Power on reset. No display.
2	Function set RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 1 0 X X		Set to 8-bit operation and select 2-line display line and 5 x 8 dot character font.
3	Display on / off control 0 0 0 0 0 0 1 1 1 0	_	Display on. Cursor appear.
4	Entry mode set 0 0 0 0 0 0 0 1 1 0	_	Increase address by one. It will shift the cursor to the right when writing to the DD RAM / CG RAM. Now the display has no shift.
5	Write data to CG RAM / DD RAM 1 0 0 1 0 1 0 1 1 1	W_	Write " W ". The cursor is incremented by one and shifted to the right.
6	:	:	:
7	Write data to CG RAM / DD RAM 1 0 0 1 0 0 0 1 0 1	WELCOME_	Write " E ". The cursor is incremented by one and shifted to the right.
8	Set DD RAM address 0 0 1 1 0 0 0 0 0 0	WELCOME _	It sets DD RAM's address. The cursor is moved to the beginning position of the 2nd line.
9	Write data to CG RAM / DD RAM 1 0 0 1 0 1 0 1 0 0	WELCOME T_	Write " T ". The cursor is incremented by one and shifted to the right.
10	:	:	:
11	Write data to CG RAM / DD RAM 1 0 0 1 0 1 0 1 0 0	WELCOME TO PART_	Write " T ". The cursor is incremented by one and shifted to the right.

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No.	Instruction	Display	Operation
12	Entry mode set 0 0 0 0 0 0 0 1 1 1	WELCOME TO PART_	When writing, it sets mode for the display shift.
13	Write data to CG RAM / DD RAM 1 0 0 1 0 1 1 0 0 1	ELCOME O PARTY_	Write " Y ". The cursor is incremented by one and shifted to the right.
14	:	:	:
15	Return home 0 0 0 0 0 0 0 0 1 0	WELCOME TO PARTY	Both the display and the cursor return to the original position (address 0).

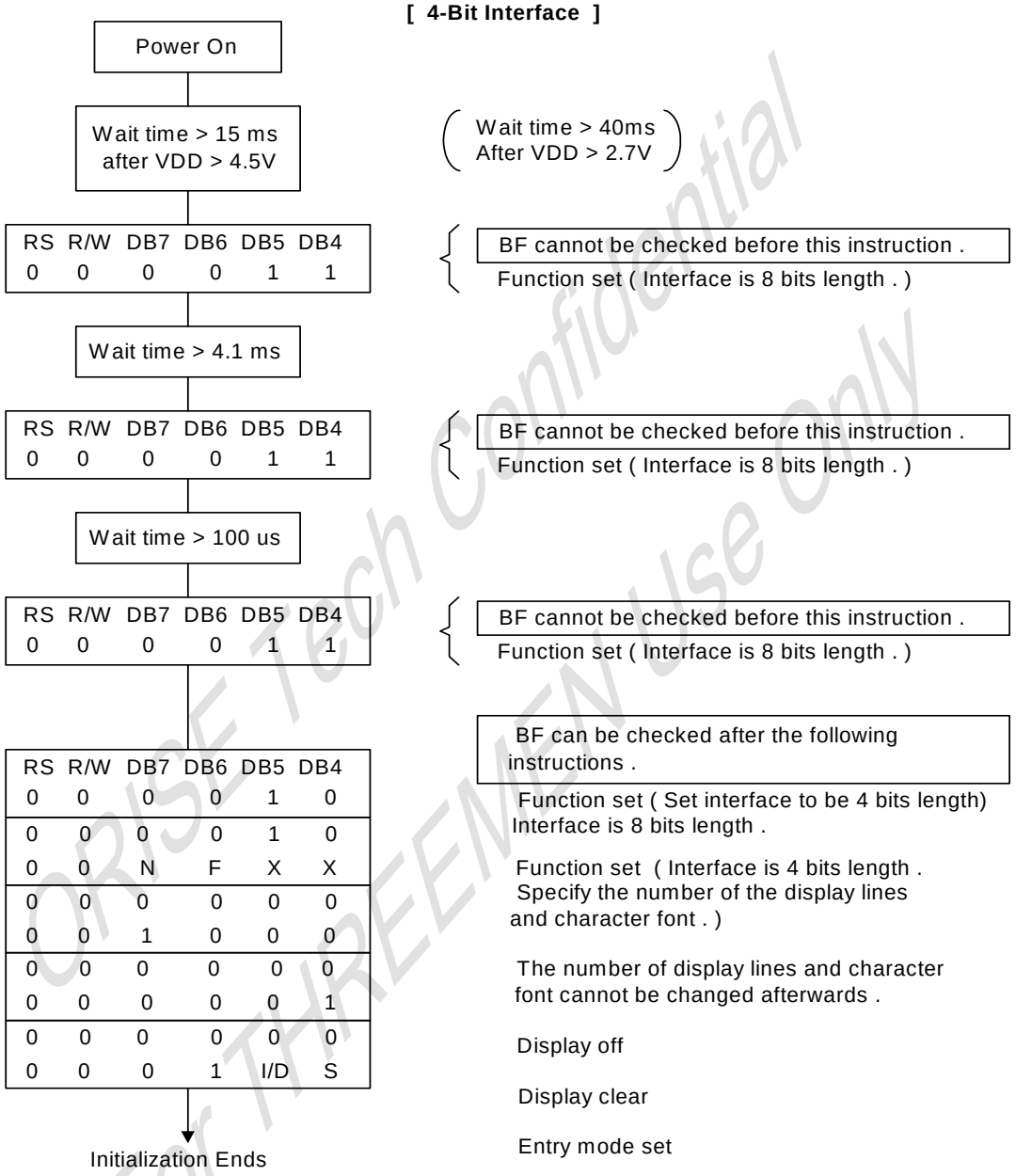
7.7. Reset Function

At power on, SPLC780D1 starts the internal auto-reset circuit and executes the initial instructions. The initial procedures are shown as follows:



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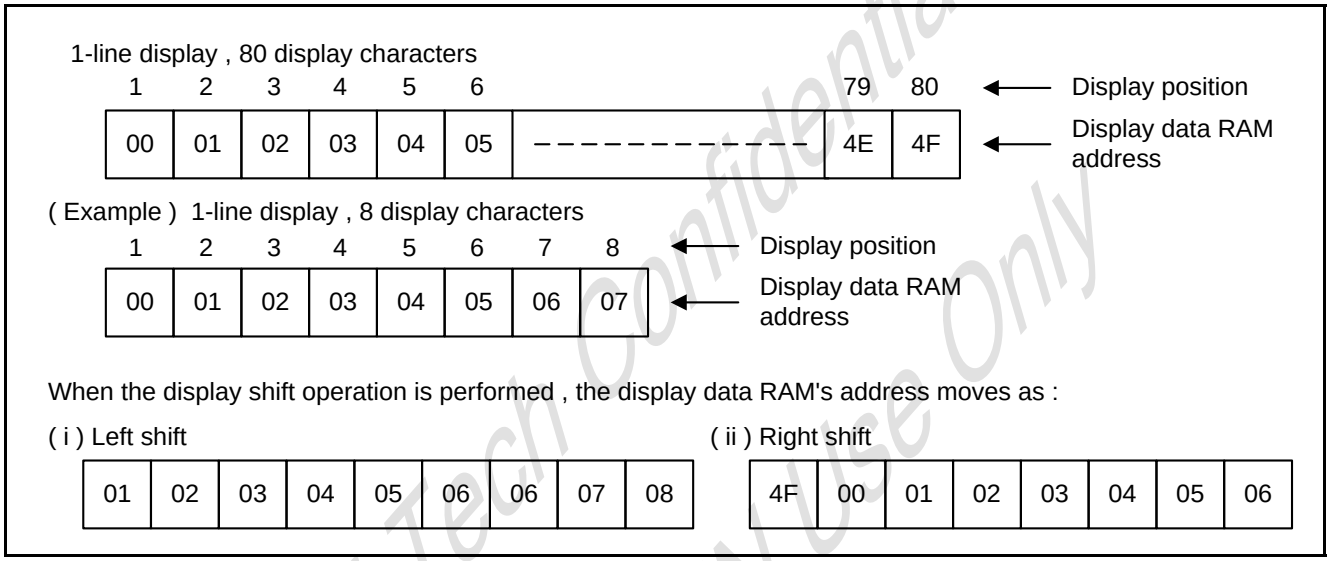
[4-Bit Interface]



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7.8. Display Data RAM (DD RAM)

The 80-bit DD RAM is normally used for storing display data. Those DD RAM not used for display data can be used as general data RAM. Its address is configured in the Address Counter. The relationships between Display Data RAM Address and LCD′s position are depicted as follows.



7.9. Timing Generation Circuit

The timing generating circuit is able to generate timing signals to the internal circuits. In order to prevent the internal timing interface, the MPU access timing and the RAM access timing are generated independently.

7.10. LCD Driver Circuit

Total of 16 commons and 40 segments signal drivers are valid in the LCD driver circuit. When a program specifies the character fonts and line numbers, the corresponding common signals output drive-waveforms and the others still output unselected waveforms.

7.11. Character Generator ROM (CG ROM)

Using 8-bit character code, the character generator ROM generates 5 x 8 dots or 5 x 10 dots character patterns. It also can generate 192's 5 x 8 dots character patterns and 64's 5 x 10 dots character patterns.

7.12. Character Generator RAM (CG RAM)

Users can easily change the character patterns in the character generator RAM through program. It can be written to 5 x 8 dots, 8-character patterns or 5 x 10 dots for 4-character patterns.

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The following diagram shows the SPLC780D1 character patterns:

Correspondence between Character Codes and Character Patterns.

Lower 4-bit (D0 to D3) of Character Code (Hexadecimal)	Higher 4-bit (D4 to D7) of Character Code (Hexadecimal)															
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	CG RAM (1)															
1	CG RAM (2)															
2	CG RAM (3)															
3	CG RAM (4)															
4	CG RAM (5)															
5	CG RAM (6)															
6	CG RAM (7)															
7	CG RAM (8)															
8	CG RAM (1)															
9	CG RAM (2)															
A	CG RAM (3)															
B	CG RAM (4)															
C	CG RAM (5)															
D	CG RAM (6)															
E	CG RAM (7)															
F	CG RAM (8)															

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The relationships between Character Generator RAM Addresses, Character Generator RAM Data (character patterns), and Character Codes are depicted as follows:

7.12.1. 5 x 8 dot character patterns

Character Code (DD RAM Data)								CG RAM Address						Character Patterns (CG RAM Data)								
b7	b6	b5	b4	b3	b2	b1	b0	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0	
0	0	0	0	X	0	0	0	0	0	0	0	0	0	X	X	X	1	1	1	1	1	Character Pattern Example (1)
											0	0	1				0	0	1	0	0	
											0	1	0				0	0	1	0	0	
											0	1	1				0	0	1	0	0	
											1	0	0				0	0	1	0	0	
											1	0	1				0	0	1	0	0	
											1	1	0				0	0	1	0	0	Cursor Position
											1	1	1				0	0	0	0	0	←
0	0	0	0	X	0	0	1	0	0	1	0	0	0	X	X	X	0	1	1	1	0	Character Pattern Example (2)
											0	0	1				0	0	1	0	0	
											0	1	0				0	0	1	0	0	
											0	1	1				0	0	1	0	0	
											1	0	0				0	0	1	0	0	
											1	0	1				0	0	1	0	0	
											1	1	0				0	1	1	1	0	
											1	1	1				0	0	0	0	0	

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Note1: ▨ It means that the bit0~2 of the character code correspond to the bit3~5 of the CG RAM address.

Note2: ▤ These areas are not used for display, but can be used for the general data RAM.

Note3: When all of the bit4-7 of the character code are 0, CG RAM character patterns are selected.

Note4: " 1 ": Selected, " 0 " : No selected , " X " : Do not care (0 or 1).

Note5: For example (1), set character code (b2 = b1 = b0 = 0, b3 = 0 or 1, b7-b4 = 0) to display " T ". That means character code (00) 16,and (08) 16 can display " T " character.

Note6: The bits 0-2 of the character code RAM is the character pattern line position. The 8th line is the cursor position and display is formed by logical OR with the cursor.

7.12.2. 5 X 10 dot character patterns

Character Code (DD RAM Data)								CG RAM Address						Character Patterns (CG RAM Data)							
b7	b6	b5	b4	b3	b2	b1	b0	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	X	0	0	X	0	0	0	0	0	0				1	0	0	0	1
										0	0	0	1				1	0	0	0	1
										0	0	1	0				1	0	0	0	1
										0	0	1	1				1	0	0	0	1
										0	1	0	0				1	0	0	0	1
										0	1	0	1	X	X	X	1	0	0	0	1
										0	1	1	0				1	0	0	0	1
										0	1	1	1				1	0	0	0	1
										1	0	0	0				1	0	0	0	1
										1	0	0	1				1	1	1	1	1
										1	0	1	0				0	0	0	0	0
										1	0	1	1								
										1	1	0	0								
										1	1	0	1	X	X	X	X	X	X	X	X
										1	1	1	0								
										1	1	1	1								

Character Pattern Example (1)

Cursor Position

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Note1: ▨ It means that the bit1~2 of the character code correspond to the bit4~5 of the CG RAM address.

Note2: ▤ These areas are not used for display, but can be used for the general data RAM.

Note3: When all of the bit4-7 of the character code are 0, CG RAM character patterns are selected.

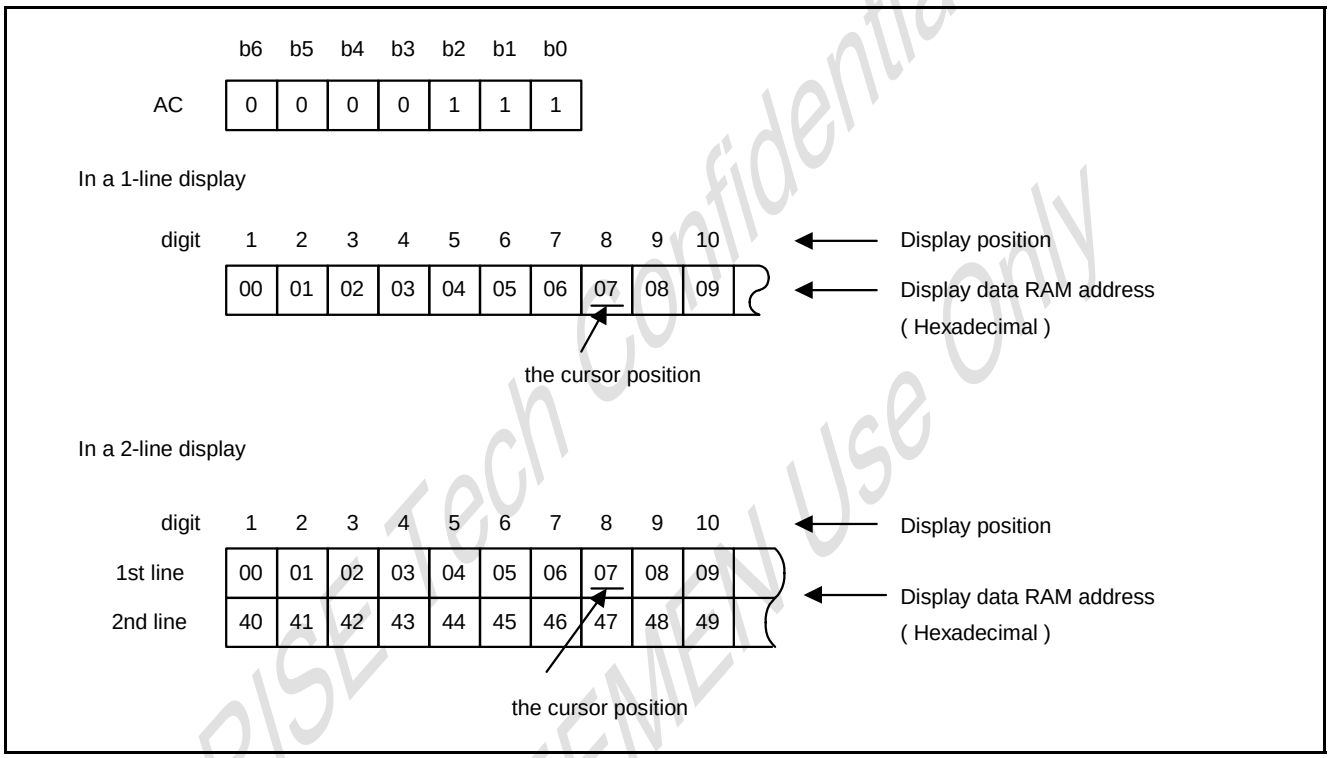
Note4: " 1 ": Selected, " 0 ": No selected, " X ": Do not care (0 or 1).

Note5: For example (1), set character code (b2 = b1 = 0, b3 = b0 = 0 or 1, b7-b4 = 0) to display " U ". That means all of the character codes (00) 16, (01) 16, (08) 16,and (09) 16 can display " U " character.

Note6: The bits 0-3 of the character code RAM is the character pattern line position. The 11th line is the cursor position and display is formed by logical OR with the cursor.

7.13. Cursor/Blink Control Circuit

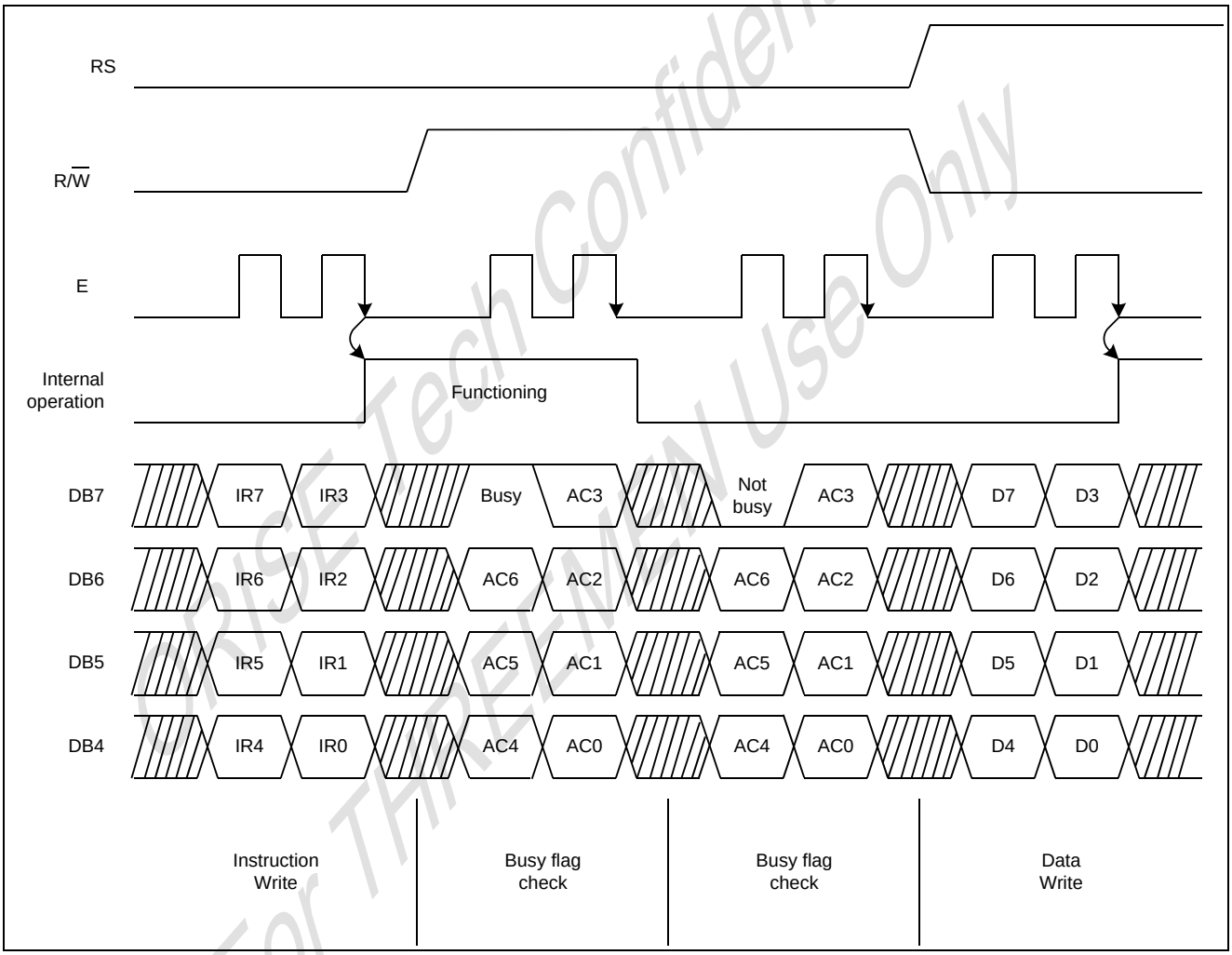
This circuit generates the cursor or blink in the cursor / blink control circuit. The cursor or the blink appears in the digit at the Display Data RAM Address defined in the Address Counter. When the Address Counter is (07) 16, the cursor position is shown as belows:



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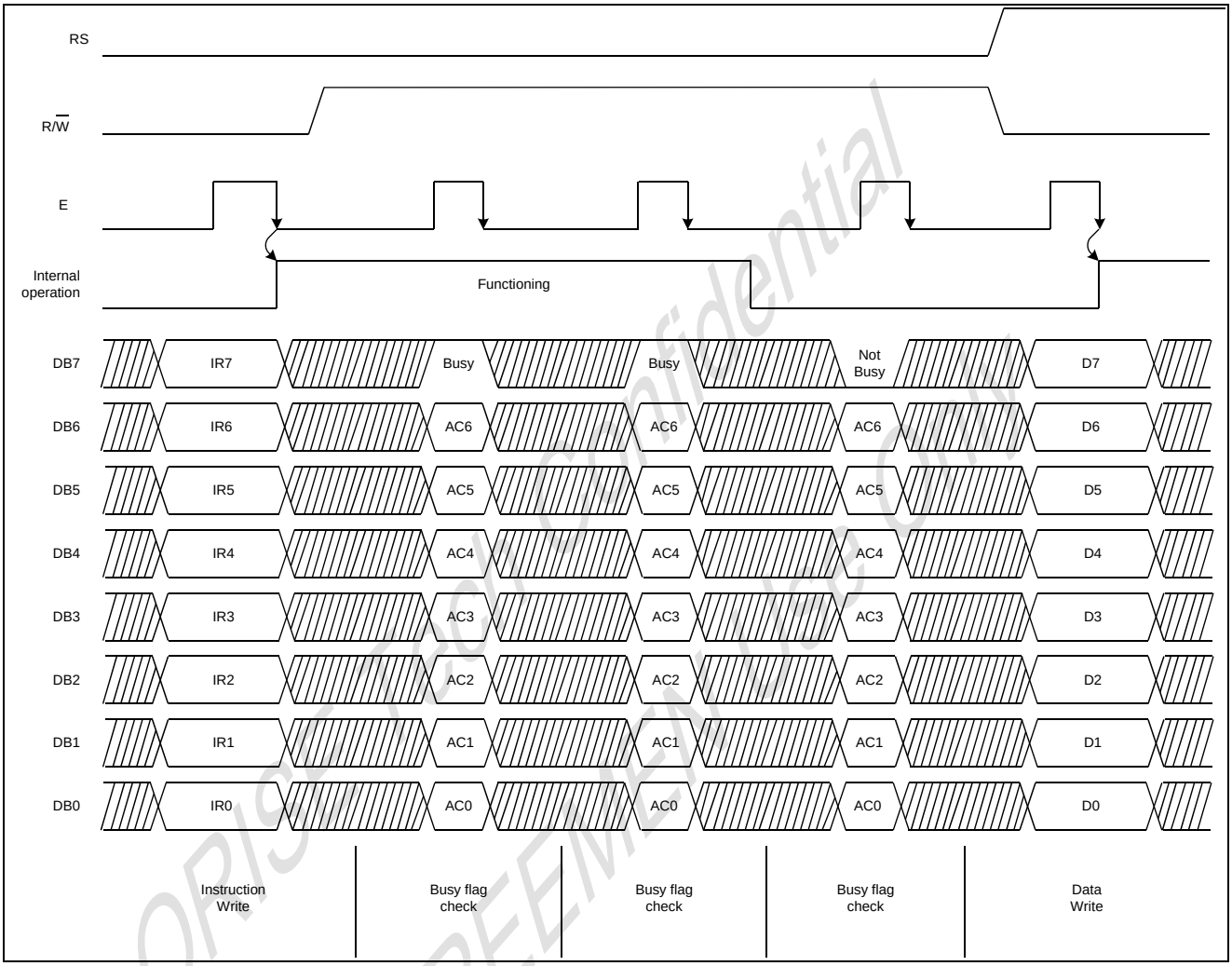
7.14. Interfacing to MPU

There are two types of data operations: 4-bit and 8-bit operations. Using 4-bit MPU, the interfacing 4-bit data is transferred by 4-busline (DB4 to DB7). Thus, DB0 to DB3 bus lines are not used. Using 4-bit MPU to interface 8-bit data requires two times transferring. First, the higher 4-bit data is transferred by 4-busline (for 8-bit operation, DB7 to DB4). Secondly, the lower 4-bit data is transferred by 4-busline (for 8-bit operation, DB3 to DB0). For 8-bit MPU, the 8-bit data is transferred by 8-buslines (DB0 to DB7).



Example of 4-bit Data Transfer Timing Sequence

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Example of 8-bit Data Transfer Timing Sequence

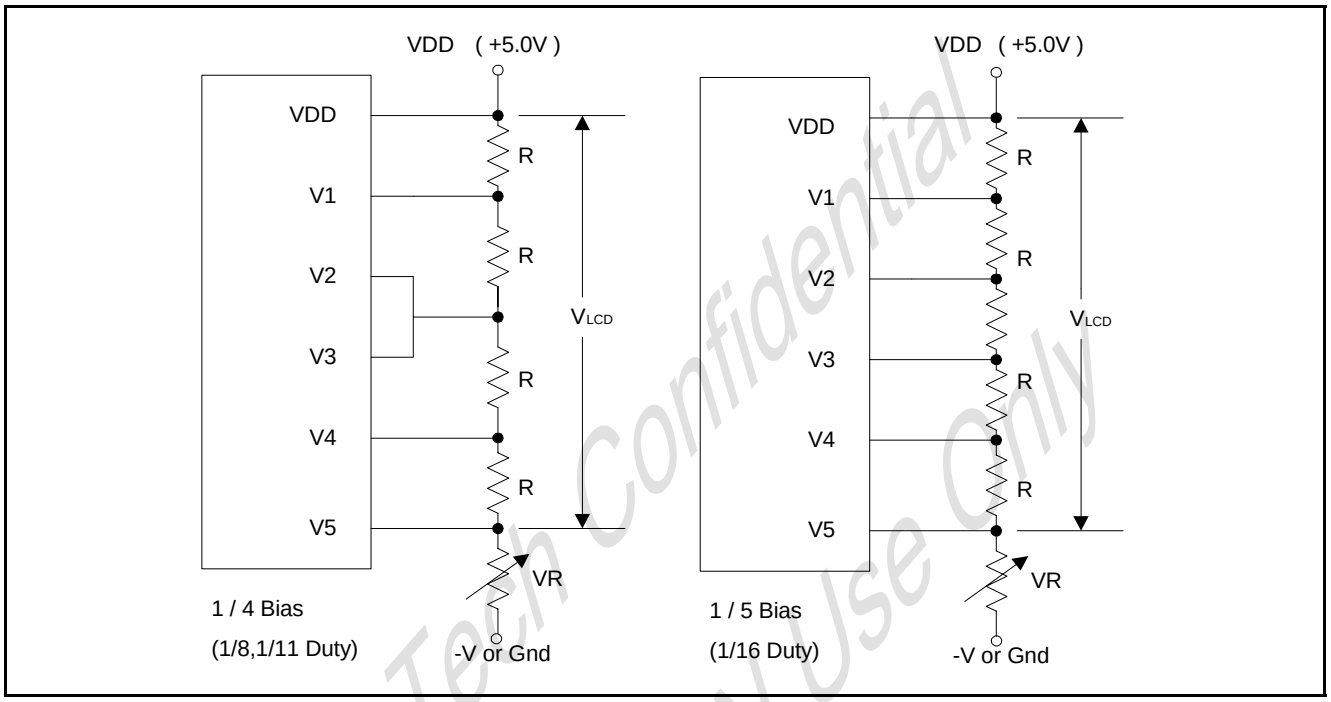
7.15. Supply Voltage for LCD Drive

Different voltages can be supplied to SPLC780D1's pins (V5 - 1) for obtaining LCD drive-waveform. The relationships between bias, duty factor and supply voltages are shown as belows:

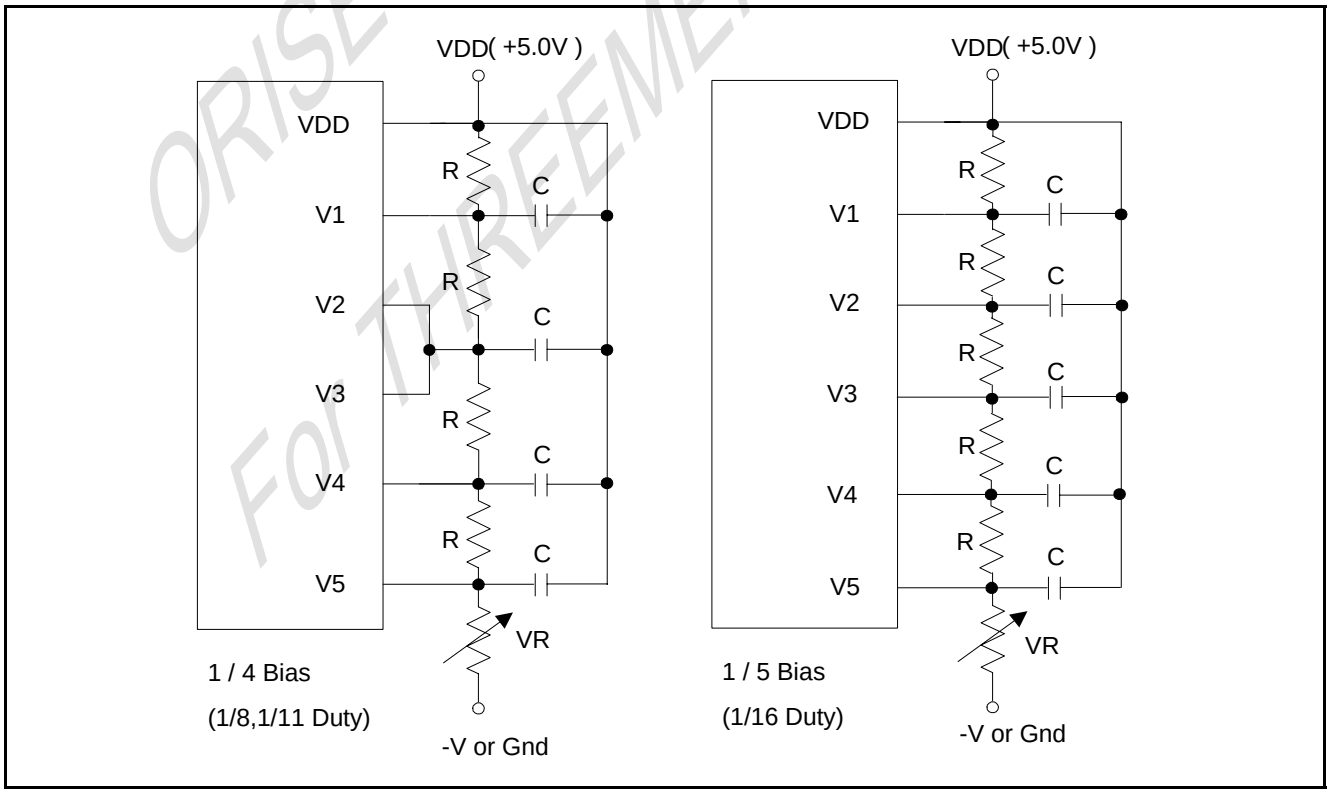
Supply Voltage \ Duty Factor	1/8, 1/11	1/16
	1/4	1/5
V1	VDD – 1/4 V_{LCD}	VDD – 1/5 V_{LCD}
V2	VDD – 1/2 V_{LCD}	VDD – 2/5 V_{LCD}
V3	VDD – 1/2 V_{LCD}	VDD – 3/5 V_{LCD}
V4	VDD – 3/4 V_{LCD}	VDD – 4/5 V_{LCD}
V5	VDD – V_{LCD}	VDD – V_{LCD}

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7.15.1. The power connections for LCD (1/4 Bias, 1/5 Bias) are shown belows:



The bypass-capacitor improves the LCD display quality.



The bias voltage must have the following relations:

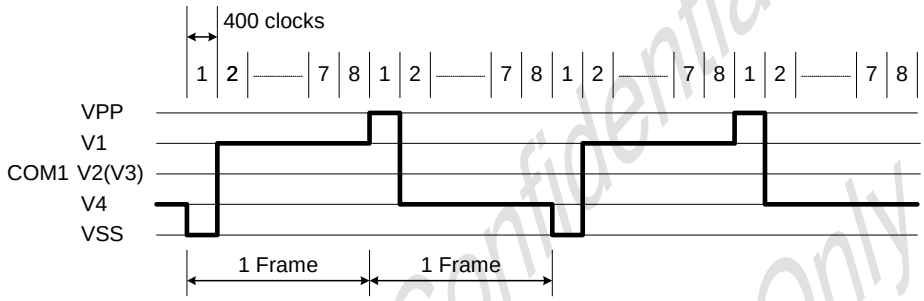
VDD > V1 > V2 ≧ V3 > V4 > V5.

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7.15.2. The relationship between LCD frame's frequency and oscillator's frequency.

(Assume the oscillation frequency is 250KHz, 1 clock cycle time = 4.0μs)

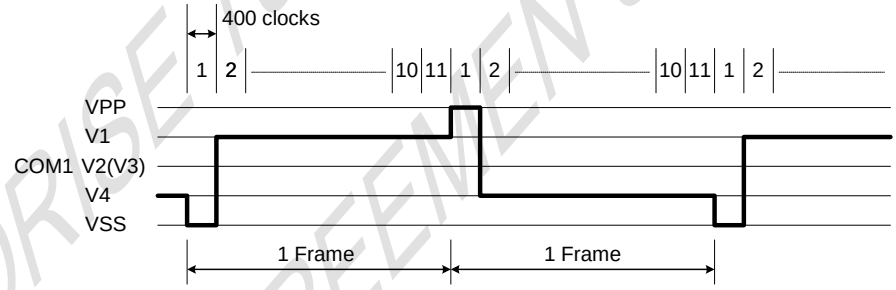
7.15.2.1. 1/8 Duty, TYPE-B waveform



1 frame = 4(μs) x 400 x 8 = 12800(μs) = 12.8ms

$$\text{Frame frequency} = \frac{1}{12.8(\text{ms})} = 78.1(\text{Hz})$$

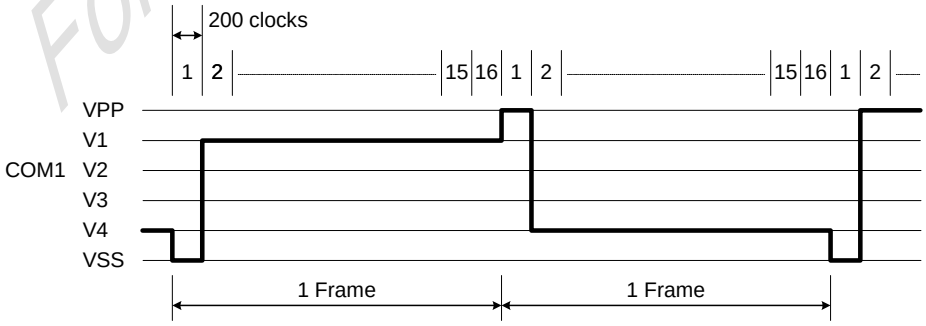
7.15.2.2. 1/11 Duty, TYPE-B waveform



1 frame = 4(μs) x 400 x 11 = 17600(μs) = 17.6ms

$$\text{Frame frequency} = \frac{1}{17.6(\text{ms})} = 56.8(\text{Hz})$$

7.15.2.3. 1/16 Duty, TYPE-B waveform



1 frame = 4(μs) x 200 x 16 = 12800(μs) = 12.8ms

$$\text{Frame frequency} = \frac{1}{12.8(\text{ms})} = 78.1(\text{Hz})$$

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7.16. REGISTER --- IR (Instruction Register) and DR (Data Register)

SPLC780D1 contains two 8-bit registers: Instruction Register (IR) and Data Register (DR). Using combinations of the RS pin and the R/W pin selects the IR and DR, see below:

RS	R/W	Operation
0	0	IR write (Display clear, etc.)
0	1	Read busy flag (DB7) and Address Counter (DB0 - DB6)
1	0	DR write (DR to Display data RAM or Character generator RAM)
1	1	DR read (Display data RAM or Character generator RAM to DR)

The IR can be written by MPU, but it cannot be read by MPU.

7.17. Busy Flag (BF)

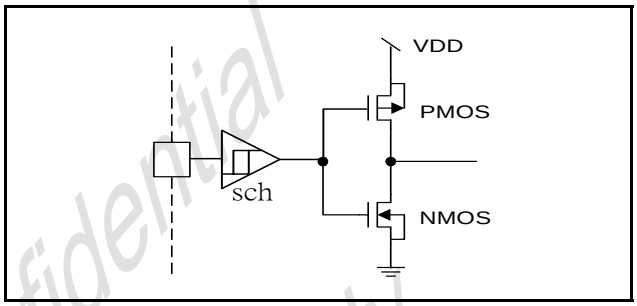
When RS = 0 and R/W = 1, the busy flag is output to DB7. As the busy flag =1, SPLC780D1 is in busy state and does not accept any instruction until the busy flag = 0.

7.18. Address Counter (AC)

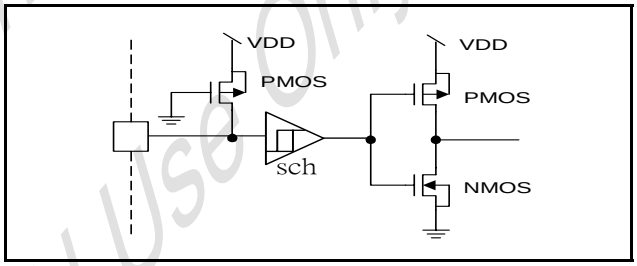
The Address Counter assigns addresses to Display Data RAM and Character Generator RAM. When an instruction for address is written in IR, the address information is sent from IR to AC. After writing to/reading from Display Data RAM or Character Generator RAM, AC is automatically incremented by one (or decremented by one). The contents of AC are output to DB0 - DB6 when RS = 0 and R/W = 1.

7.19. I/O Port Configuration

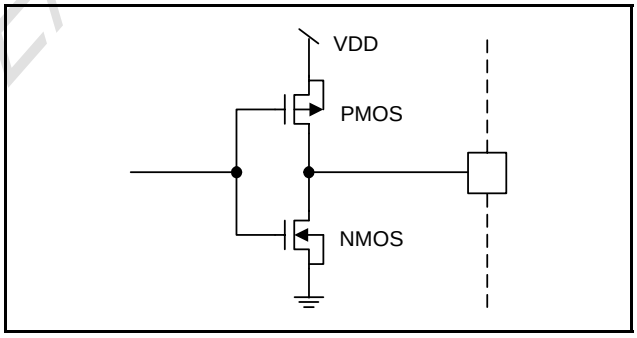
7.19.1. Input port: E



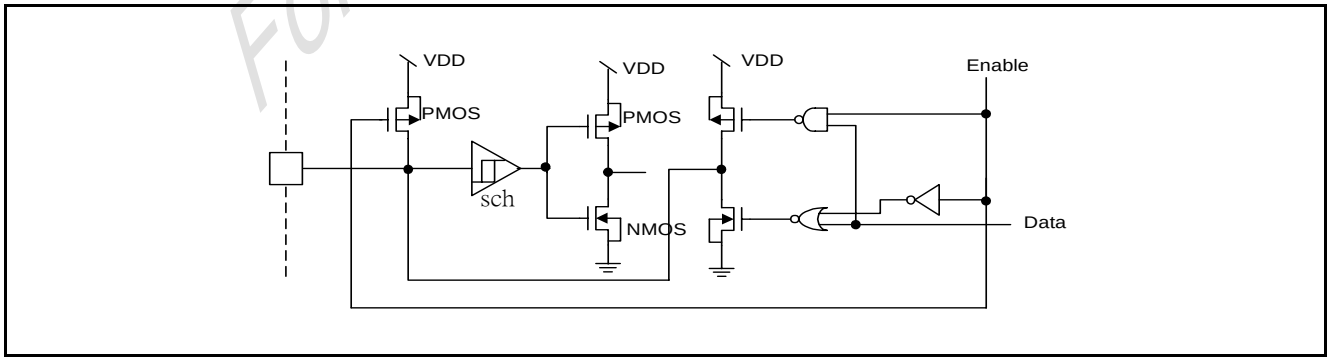
7.19.2. Input port: R/W, RS



7.19.3. Output port: CL1, CL2, M, D



7.19.4. Input / Output port: DB7 - DB0



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8. ELECTRICAL SPECIFICATIONS

8.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
Operating Voltage	VDD	-0.3V to +7.0V
Driver Supply Voltage	V_{LCD}	VDD - 10V to VDD + 0.3V
Input Voltage Range	V_{IN}	-0.3V to VDD + 0.3V
Operating Temperature	T_A	-30℃ to +80℃
Storage Temperature	T_{STO}	-55℃ to +125℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

8.2. DC Characteristics (VDD = 2.7V to 4.5V, T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Current	I_{DD}	-	0.2	0.4	mA	External clock (Note)
Input High Voltage	V_{IH1}	0.7VDD	-	VDD	V	Pins:(E, RS, R/W, DB0 - DB7)
Input Low Voltage	V_{IL1}	-0.3	-	0.55	V	
Input High Voltage	V_{IH2}	0.7VDD	-	VDD	V	Pin OSC1
Input Low Voltage	V_{IL2}	-0.2	-	0.2VDD	V	
Input High Current	I_{IH}	-1.0	-	1.0	μA	Pins: (RS, R/W, DB0 - DB7)
Input Low Current	I_{IL}	-10.0	-50	-120	μA	VDD = 3.0V
Output High Voltage (TTL)	V_{OH1}	0.75VDD	-	-	V	I_{OH} = - 0.1mA Pins: DB0 - DB7
Output Low Voltage (TTL)	V_{OL1}	-	-	0.2VDD	V	I_{OL} = 0.1mA Pins: DB0 - DB7
Output High Voltage (CMOS)	V_{OH2}	0.8VDD	-	-	V	I_{OH} = - 40μA, Pins: CL1, CL2, M, D
Output Low Voltage (CMOS)	V_{OL2}	-	-	0.2VDD	V	I_{OL} = 40μA, Pins: CL1, CL2, M, D
Driver ON Resistance (COM)	R_{COM}	-	-	20	KΩ	I_O = ±50μA, V_{LCD} = 4.0V Pins: COM1 - COM16
Driver ON Resistance (SEG)	R_{SEG}	-	-	30	KΩ	I_O = ±50μA, V_{LCD} = 4.0V Pins: SEG1 - SEG40
LCD Voltage	V_{LCD}	3.0	-	8.0	V	VDD-V5, 1/4 bias or 1/5 bias

Note: F_{OSC} = 250KHz, VDD = 3.0V, pin E = "L", RS, R/W, DB0 - DB7 are open, all outputs are no loads.

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8.3. AC Characteristics (VDD = 2.7V to 4.5V, T_A = 25℃)

8.3.1. Internal clock operation

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
OSC Frequency	F_{OSC1}	190	270	350	KHz	VDD = 3.0V, Rf = 75KΩ±2%

8.3.2. External clock operation

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
External Frequency	F_{OSC2}	125	250	350	KHz	
Duty Cycle		45	50	55	%	
Rise/Fall Time	t r, t f	-	-	0.2	μs	

8.3.3. Write mode (Writing data from MPU to SPLC780D1)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
E Cycle Time	t_C	1000	-	-	ns	Pin E
E Pulse Width	t_{PW}	450	-	-	ns	Pin E
E Rise/Fall Time	t_R, t_F	-	-	25	ns	Pin E
Address Setup Time	t_{SP1}	60	-	-	ns	Pins: RS, R/W, E
Address Hold Time	t_{HD1}	20	-	-	ns	Pins: RS, R/W, E
Data Setup Time	t_{SP2}	195	-	-	ns	Pins: DB0 - DB7
Data Hold Time	t_{HD2}	10	-	-	ns	Pins: DB0 - DB7

8.3.4. Read mode (Reading data from SPLC780D1 to MPU)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
E Cycle Time	t_C	1000	-	-	ns	Pin E
E Pulse Width	t_W	450	-	-	ns	Pin E
E Rise/Fall Time	t_R, t_F	-	-	25	ns	Pin E
Address Setup Time	t_{SP1}	60	-	-	ns	Pins: RS, R/W, E
Address Hold Time	t_{HD1}	20	-	-	ns	Pins: RS, R/W, E
Data Output Delay Time	t_D	-	-	360	ns	Pins: DB0 - DB7
Data hold time	t_{HD2}	5.0	-	-	ns	Pin DB0 - DB7

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8.4. DC Characteristics (VDD = 4.5V to 5.5V, T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Current	I_{DD}	-	0.55	0.8	mA	External clock (Note)
Input High Voltage	V_{IH1}	2.5	-	VDD	V	Pins:(E, RS, R/W, DB0 - DB7)
Input Low Voltage	V_{IL1}	-0.3	-	0.6	V	VDD=5V
Input High Voltage	V_{IH2}	VDD-1	-	VDD	V	Pin OSC1
Input Low Voltage	V_{IL2}	-0.2	-	1.0	V	Pin OSC1
Input High Current	I_{IH}	-2.0	-	2.0	μA	Pins: (RS, R/W, DB0 - DB7)
Input Low Current	I_{IL}	-20	-125	-250	μA	VDD = 5.0V
Output High Voltage (TTL)	V_{OH1}	2.4	-	VDD	V	I_{OH} = - 0.1mA Pins: DB0 - DB7
Output Low Voltage (TTL)	V_{OL1}	-	-	0.4	V	I_{OL} = 0.1mA Pins: DB0 - DB7
Output High Voltage (CMOS)	V_{OH2}	0.9VDD	-	VDD	V	I_{OH} = - 40μA, Pins: CL1, CL2, M, D
Output Low Voltage (CMOS)	V_{OL2}	-	-	0.1VDD	V	I_{OL} = 40μA, Pins: CL1, CL2, M, D
Driver ON Resistance (COM)	R_{COM}	-	-	20	KΩ	I_O = ±50μA, V_{LCD} = 4.0V Pins: COM1 - COM16
Driver ON Resistance (SEG)	R_{SEG}	-	-	30	KΩ	I_O = ±50μA, V_{LCD} = 4.0V Pins: SEG1 - SEG40
LCD Voltage	V_{LCD}	3.0	-	8	V	VDD-V5, 1/4 bias or 1/5 bias

Note: F_{osc} = 250KHz, VDD = 5.0V, pin E = "L", RS, R/W, DB0 - DB7 are open, all outputs are no loads.

8.5. AC Characteristics (VDD = 4.5V to 5.5V, T_A = 25℃)

8.5.1. Internal clock operation

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
OSC Frequency	F_{OSC1}	190	270	350	KHz	VDD = 5.0V, Rf = 91KΩ±2%

8.5.2. External clock operation

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
External Frequency	F_{OSC2}	125	250	350	KHz	
Duty Cycle		45	50	55	%	
Rise/Fall Time	t r, t f	-	-	0.2	μs	

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8.5.3. Write mode (Writing Data from MPU to SPLC780D1)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
E Cycle Time	t_C	400	-	-	ns	Pin E
E Pulse Width	t_{PW}	150	-	-	ns	Pin E
E Rise/Fall Time	t_R, t_F	-	-	25	ns	Pin E
Address Setup Time	t_{SP1}	30	-	-	ns	Pins: RS, R/W, E
Address Hold Time	t_{HD1}	10	-	-	ns	Pins: RS, R/W, E
Data Setup Time	t_{SP2}	40	-	-	ns	Pins: DB0 - DB7
Data Hold Time	t_{HD2}	10	-	-	ns	Pins: DB0 - DB7

8.5.4. Read mode (Reading Data from SPLC780D1 to MPU)

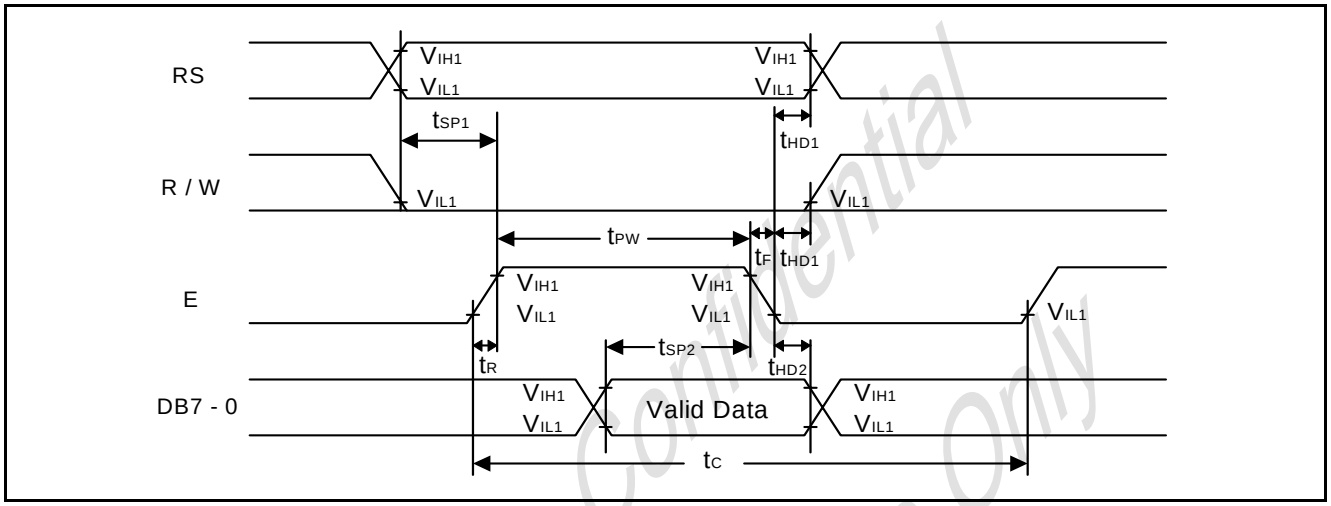
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
E Cycle Time	t_C	400	-	-	ns	Pin E
E Pulse Width	t_W	150	-	-	ns	Pin E
E Rise/Fall Time	t_R, t_F	-	-	25	ns	Pin E
Address Setup Time	t_{SP1}	30	-	-	ns	Pins: RS, R/W, E
Address Hold Time	t_{HD1}	10	-	-	ns	Pins: RS, R/W, E
Data Output Delay Time	t_D	-	-	100	ns	Pins: DB0 - DB7
Data hold time	t_{HD2}	5.0	-	-	ns	Pin DB0 - DB7

8.5.5. Interface mode with LCD Driver (SPLC100B1)

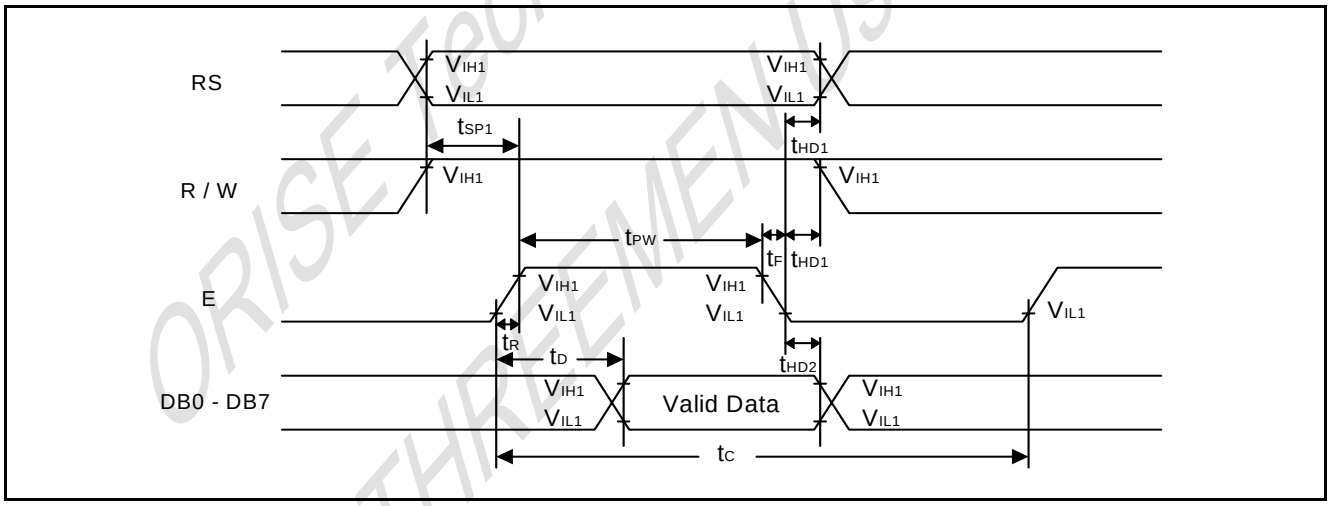
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Clock pulse width high	t_{PWH}	800	-	-	ns	Pins: CL1, CL2
Clock pulse width low	t_{PWL}	800	-	-	ns	Pins: CL1, CL2
Clock setup time	t_{CSP}	500	-	-	ns	Pins: CL1, CL2
Data setup time	t_{DSP}	300	-	-	ns	Pins: D
Data hold time	t_{HD}	300	-	-	ns	Pins: D
M delay time	t_D	-1000	-	1000	ns	Pins: M

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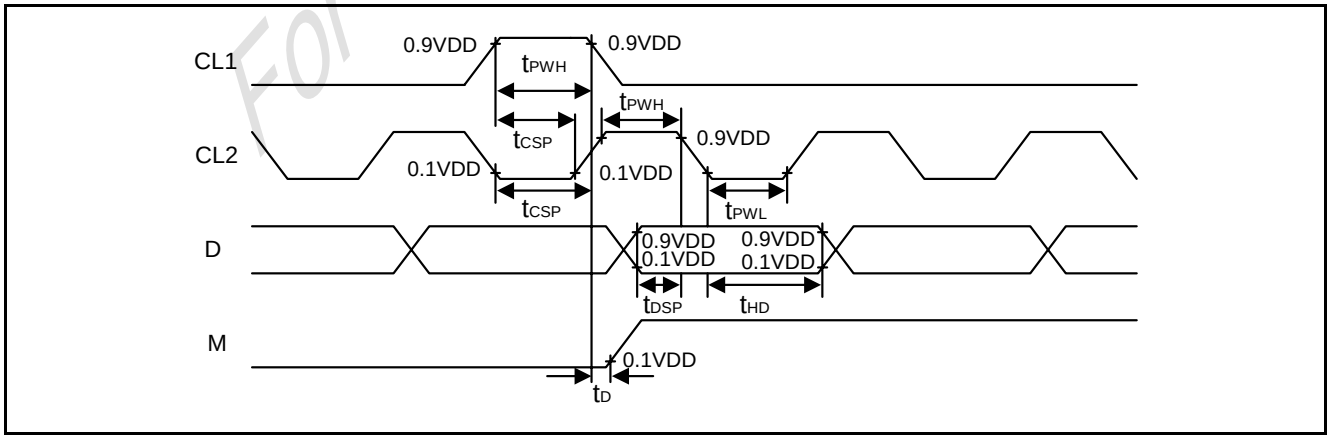
8.5.6. Write mode timing diagram (Writing Data from MPU to SPLC780D1)



8.5.7. Read mode timing diagram (Reading Data from SPLC780D1 to MPU)



8.5.8. Interface mode with SPLC100B1 timing diagram

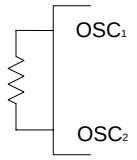


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9. APPLICATION CIRCUITS

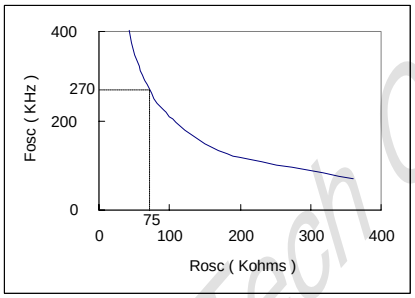
9.1. R-Oscillator

The oscillation resistor R_f is used only for the internal oscillator operation mode.

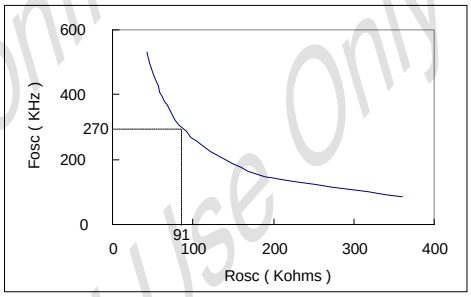


R_f : 75.0KΩ±2% (when VDD = 3.0V)
R_f : 91KΩ± 2% (when VDD = 5.0V)

Since the oscillation frequency varies depending on the OSC_1 and OSC_2 pin capacitance, the wiring length to these pins should be minimized.



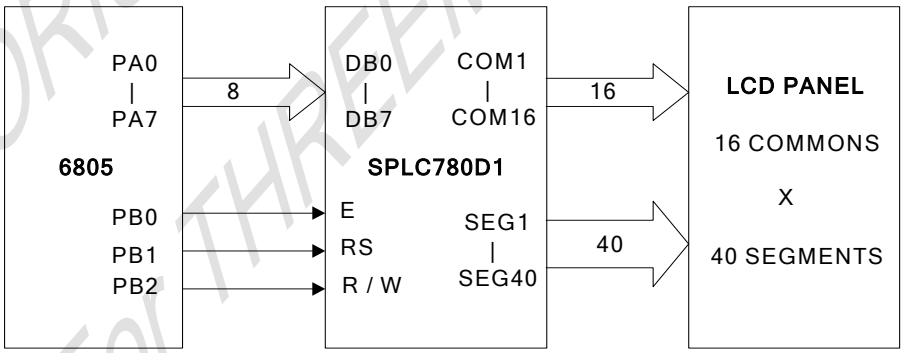
VDD = 3.0V



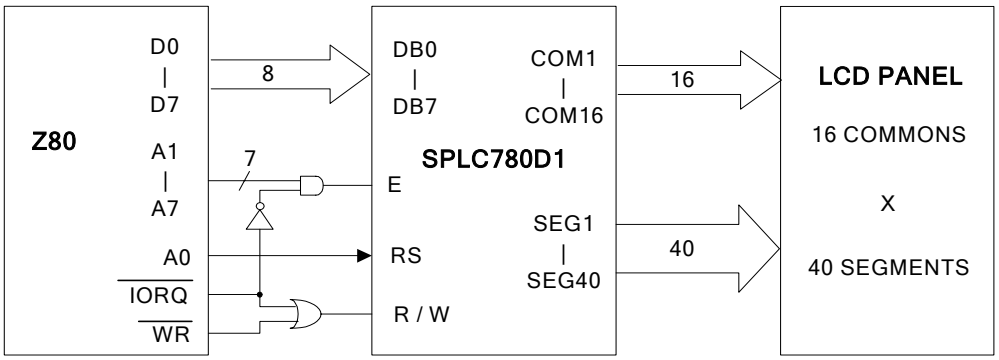
VDD = 5.0V

9.2. Interface to MPU

9.2.1. Interface to 8-bit MPU (6805)

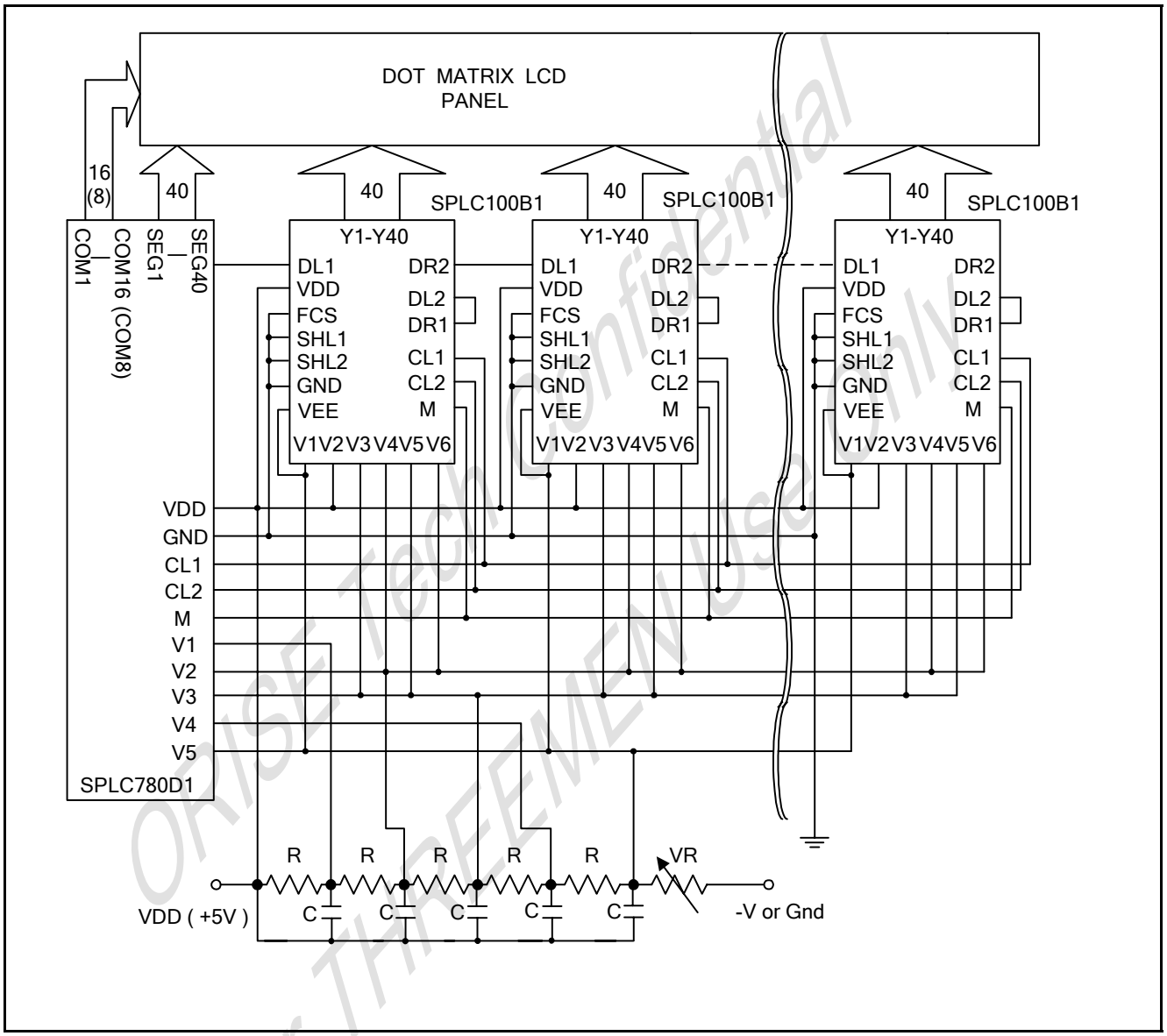


9.2.2. Interface to 8-bit MPU (Z80)



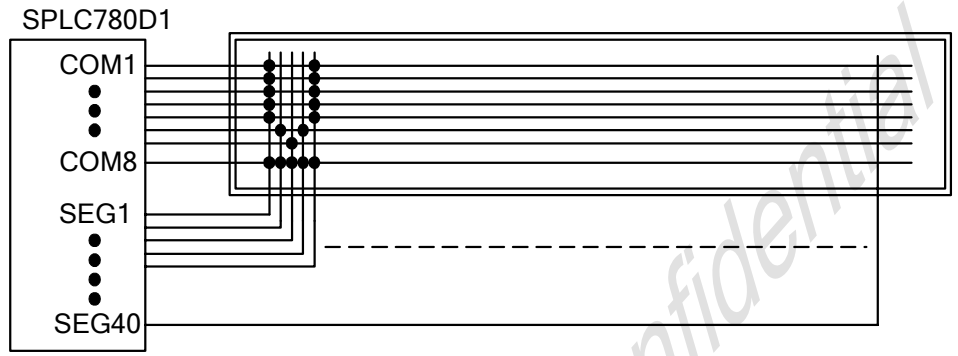
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9.3. SPLC780D1 Application Circuit

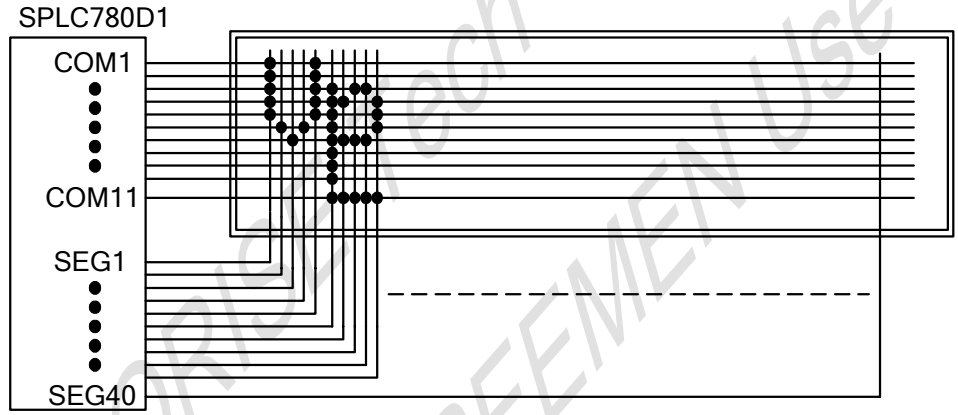


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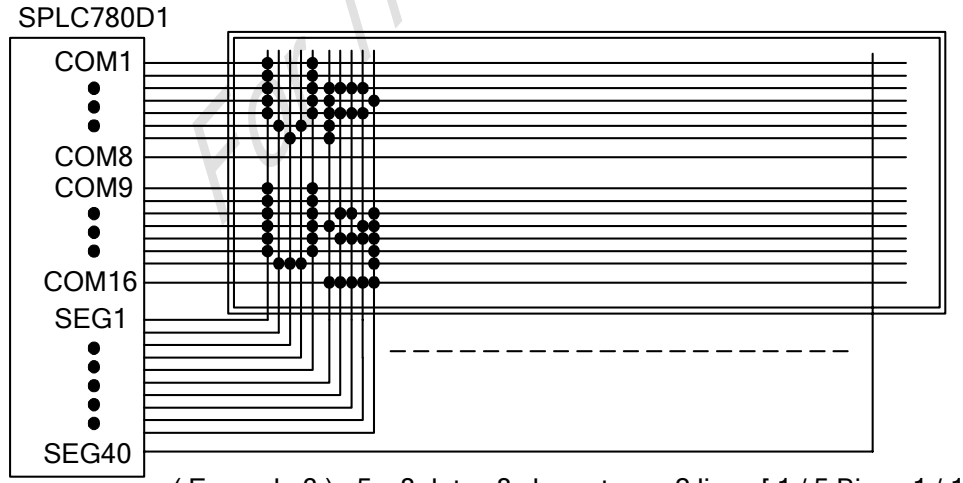
9.4. Applications for LCD



(Example 1) : 5 x 8 dots , 8 characters x 1 line [1 / 4 Bias , 1 / 8 Duty]

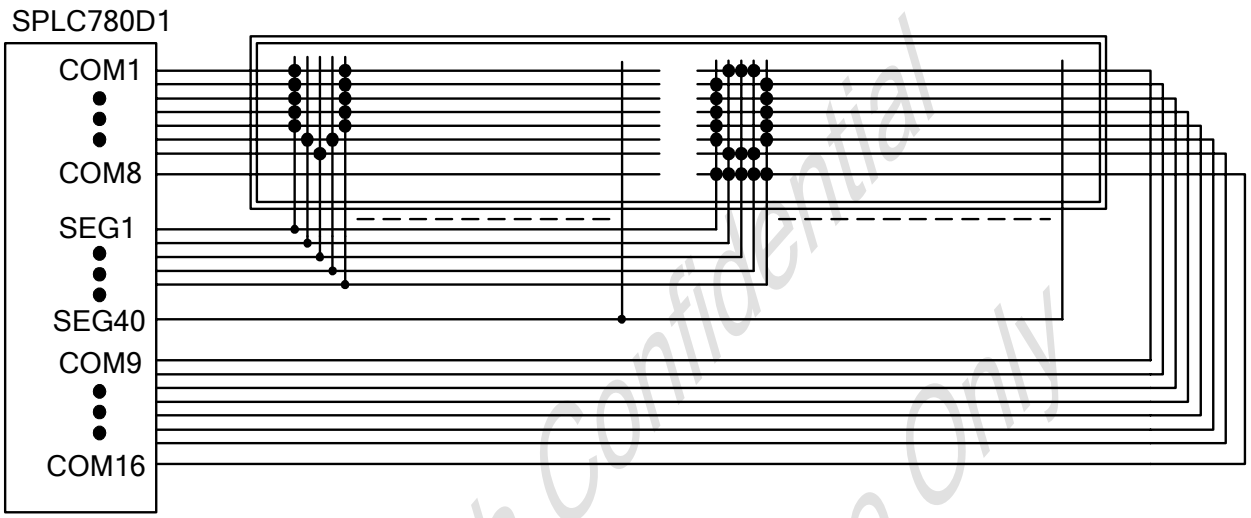


(Example 2) : 5 x 10 dots , 8 characters x 1 line [1 / 4 Bias , 1 / 11 Duty]

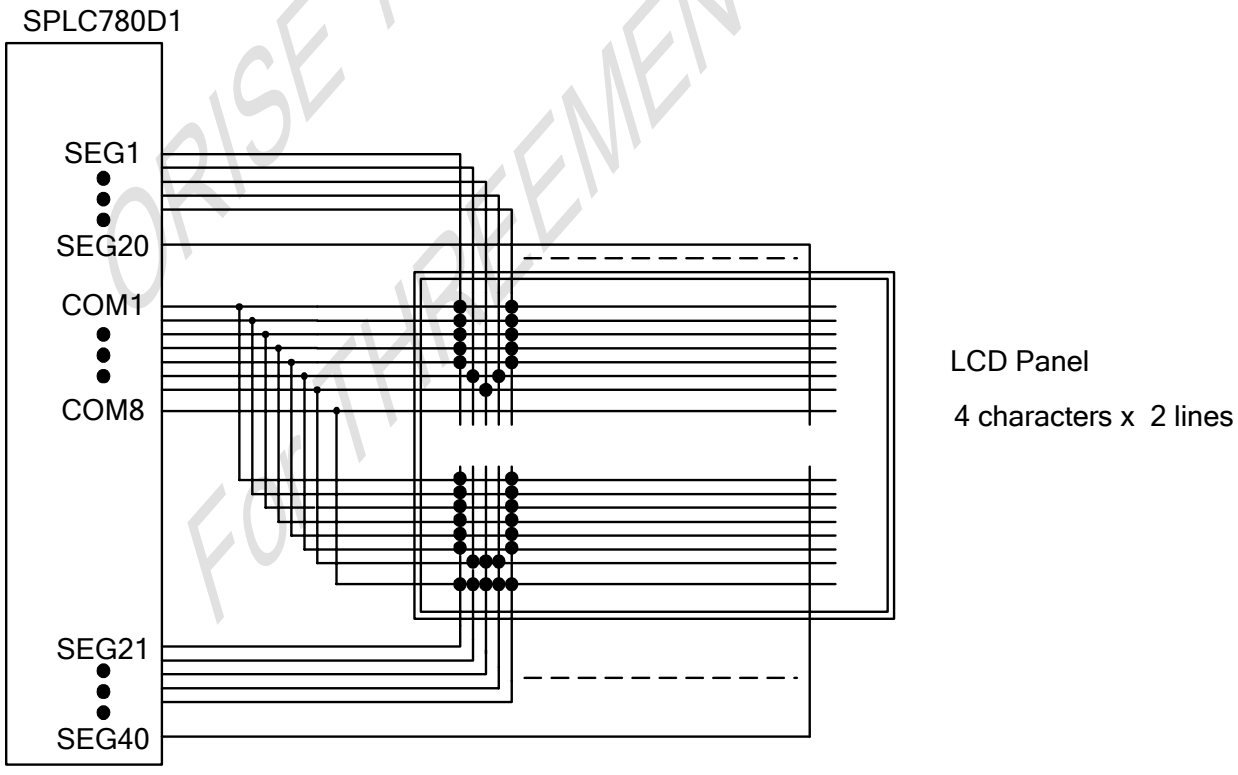


(Example 3) : 5 x 8 dots , 8 characters x 2 lines [1 / 5 Bias , 1 / 16 Duty]

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(Example 4) : 5 x 8 dots , 16 characters x 1 line [1 / 5 Bias , 1 / 16 Duty]

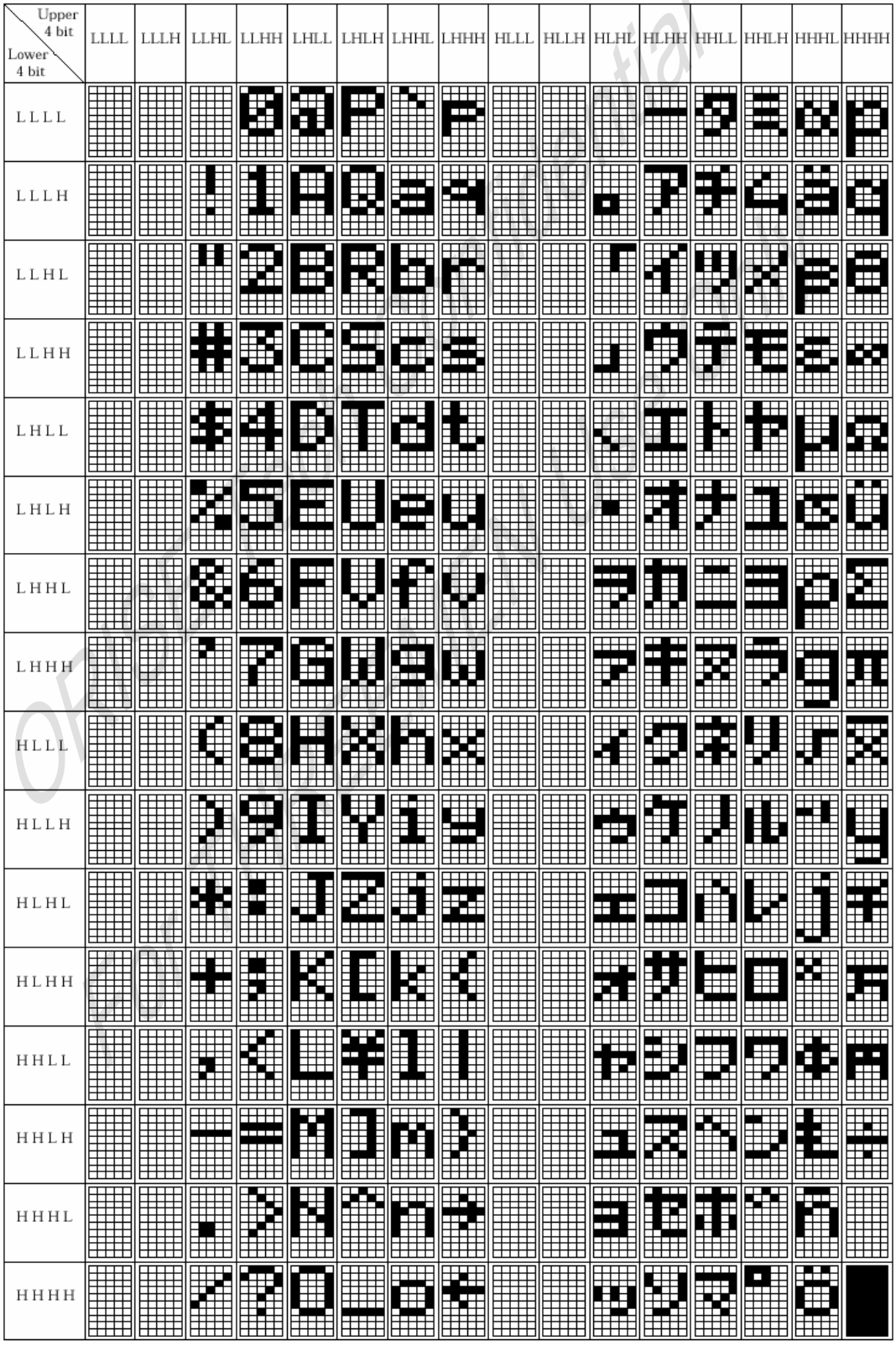


(Example 5) : 5 x 8 dots , 4 characters x 2 lines [1 / 4 Bias , 1 / 8 Duty]

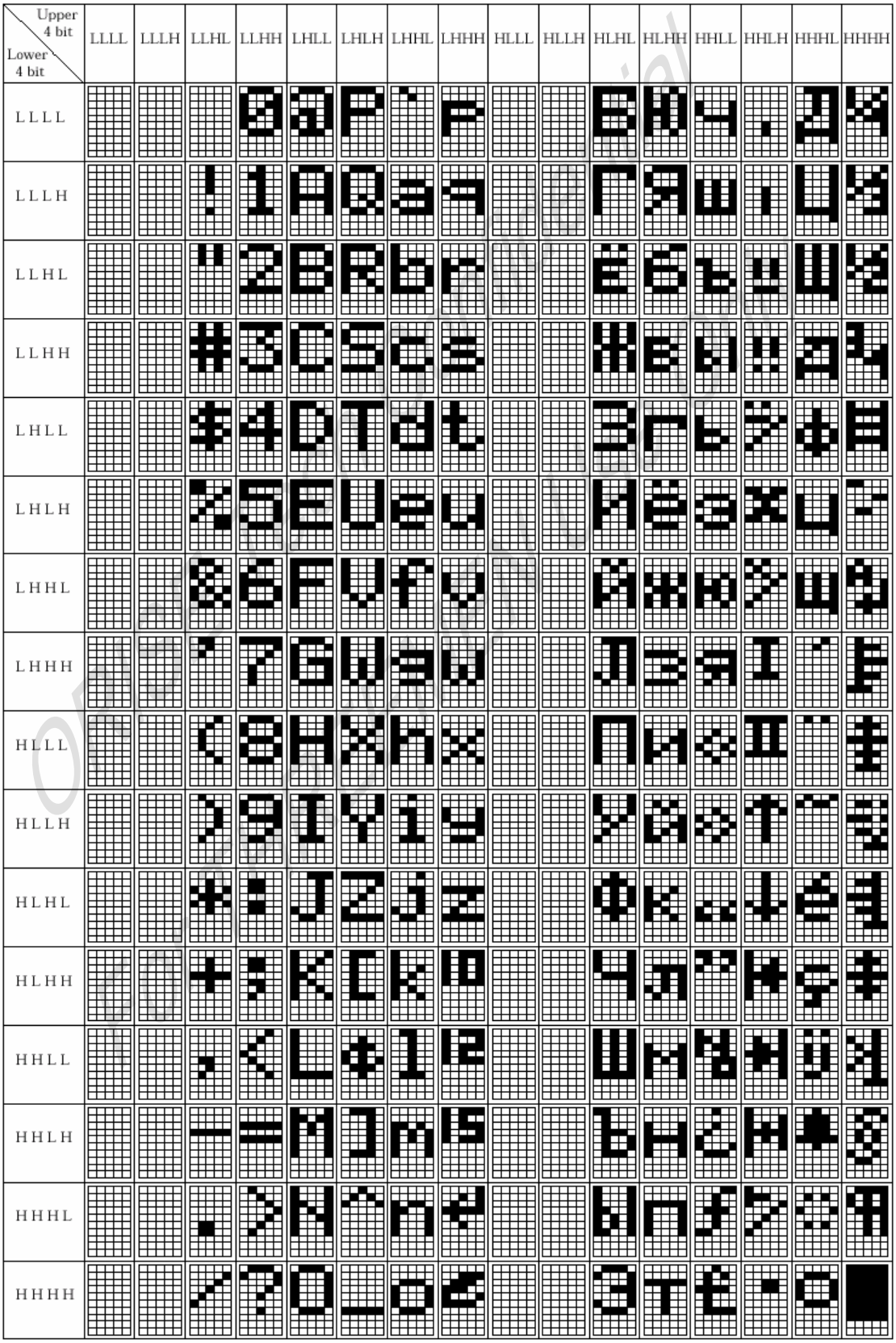
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10. CHARACTER GENERATOR ROM

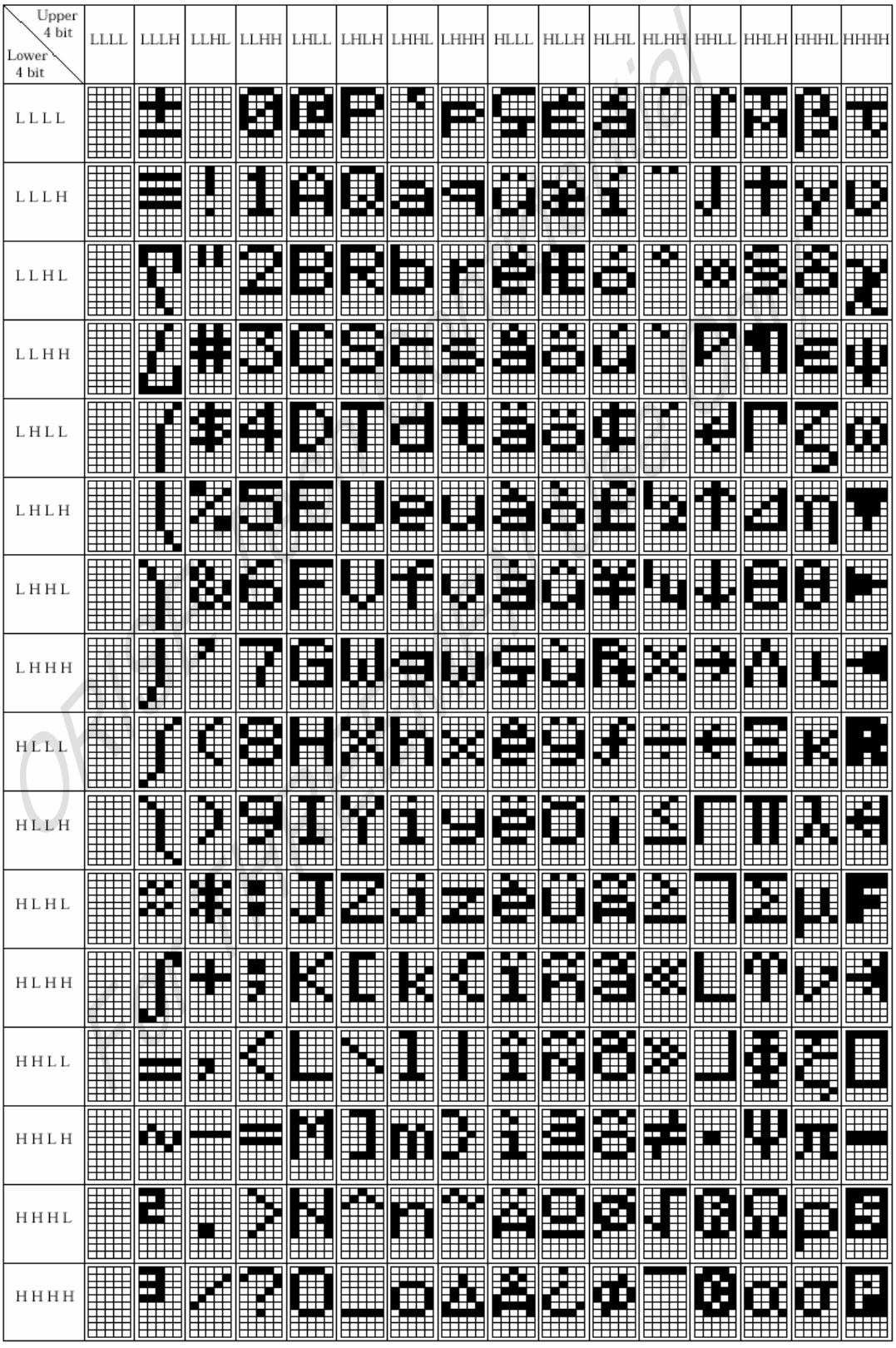
10.1. SPLC780D1 – 001A



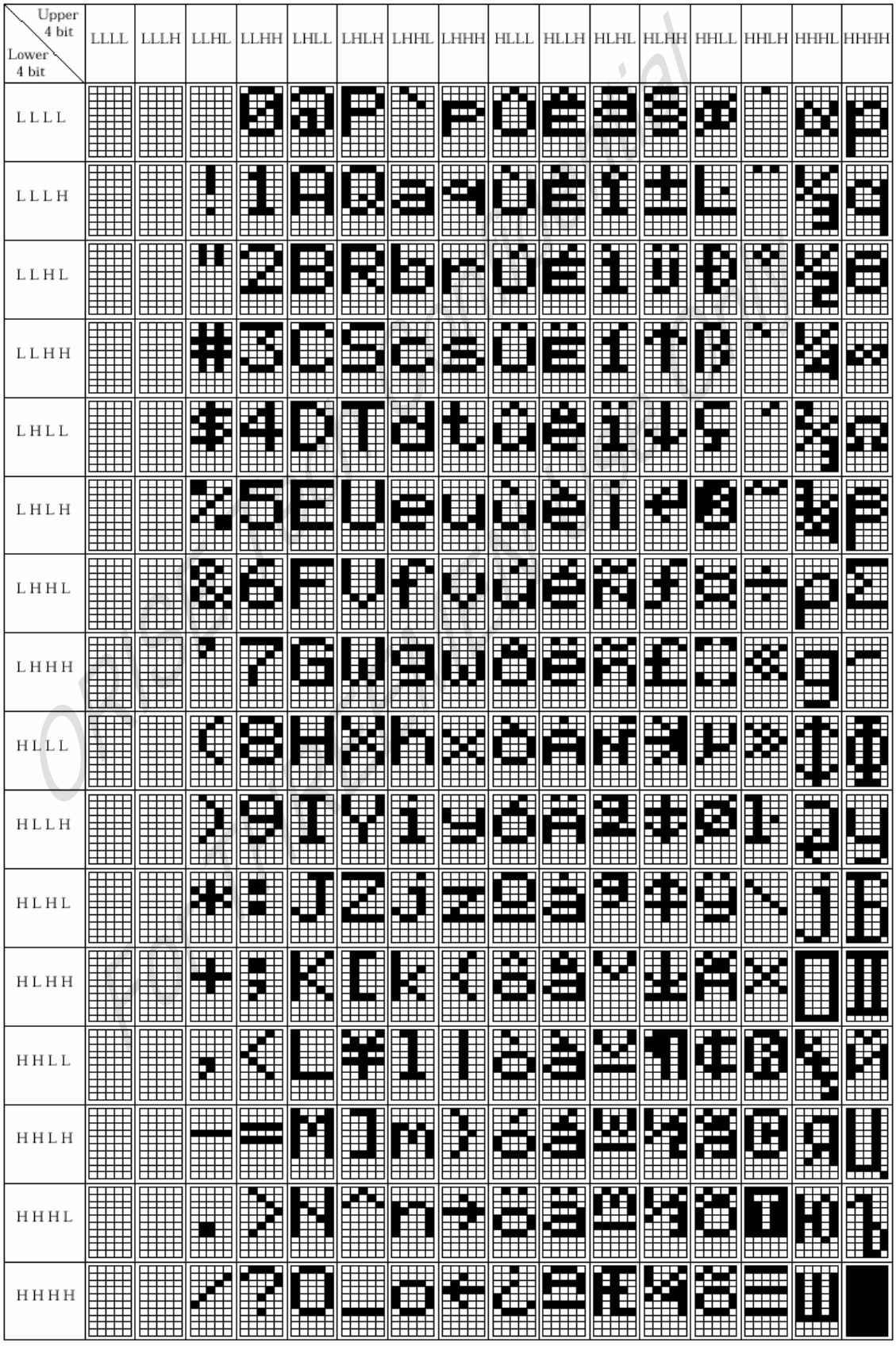
10.2. SPLC780D1 – 002A



10.3. SPLC780D1 – 003A



10.4. SPLC780D1 – 011A

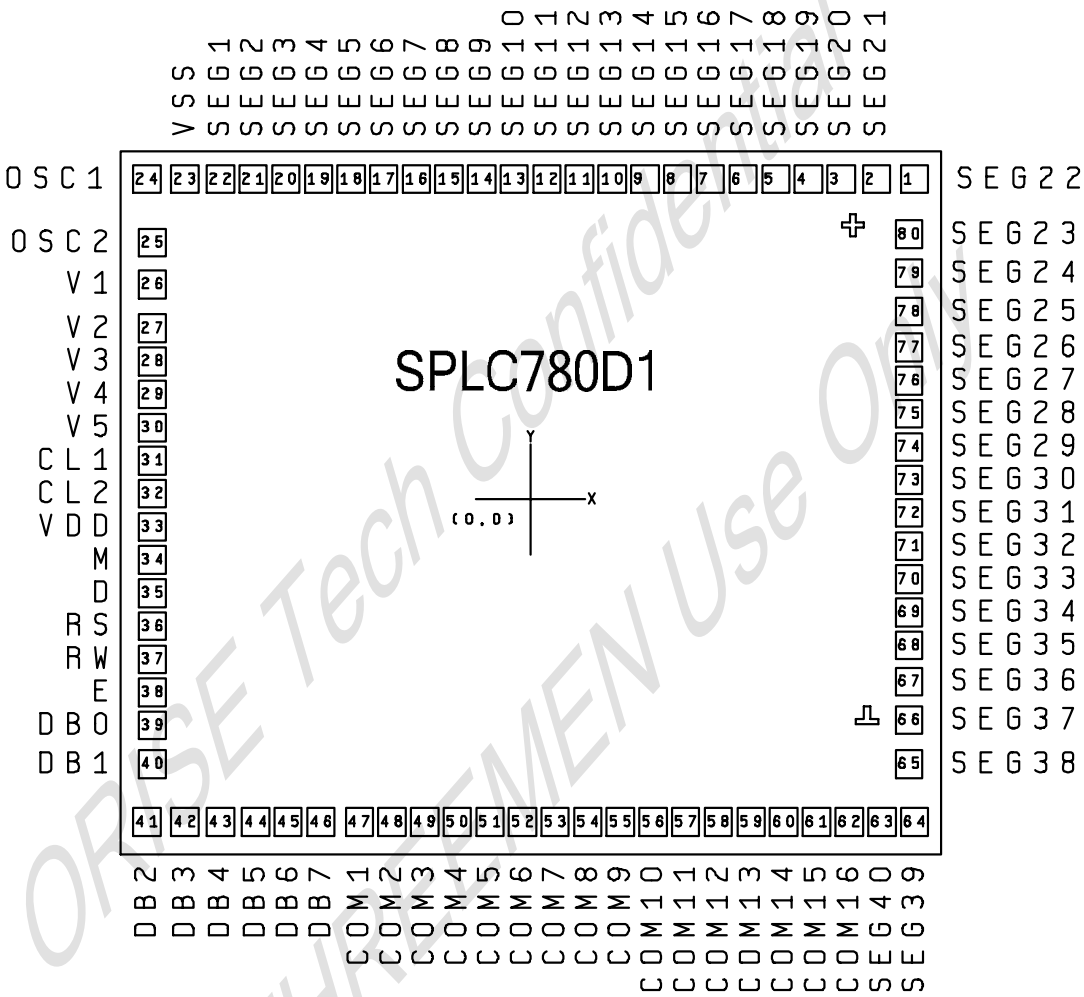


10.5. SPLC780D1 – 021A



11. PACKAGE/PAD LOCATIONS

11.1. PAD Assignment



Chip Size: 2860μm x 2450μm

PAD Size: 90μm x 90μm

This IC substrate should be connected to VDD

Note1: Chip size included scribe line.

Note2: To ensure that the IC functions properly, please bond all of VDD and VSS pins.

Note3: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

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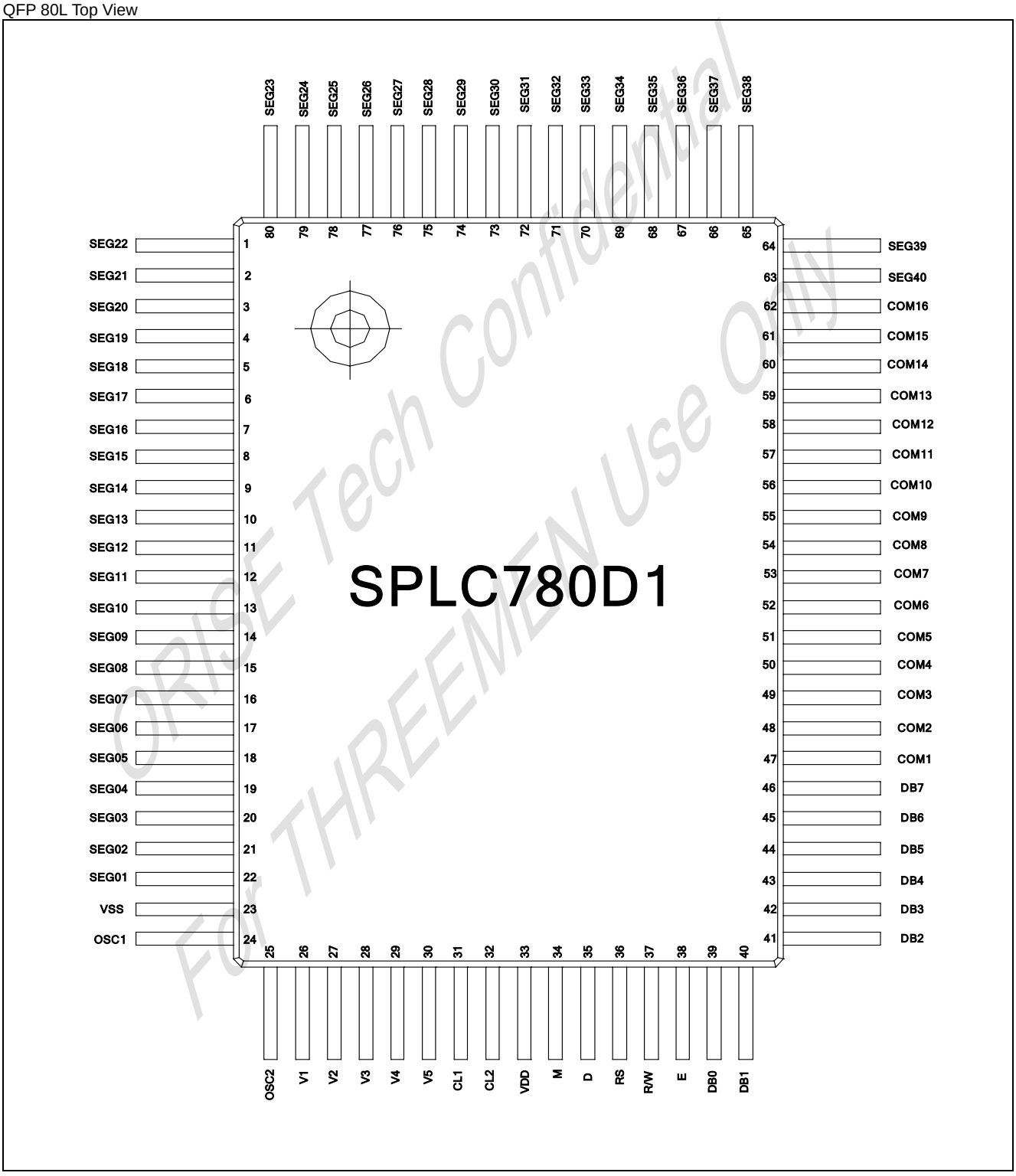
11.2. PAD Locations

PAD No.	PAD Name	X	Y	PAD No.	PAD Name	X	Y
1	SEG22	1295.0	1058.5	41	DB2	-1295.0	-1058.5
2	SEG21	1175.0	1058.5	42	DB3	-1175.0	-1058.5
3	SEG20	1055.0	1058.5	43	DB4	-1055.0	-1058.5
4	SEG19	940.0	1058.5	44	DB5	-940.0	-1058.5
5	SEG18	825.0	1058.5	45	DB6	-825.0	-1058.5
6	SEG17	715.0	1058.5	46	DB7	-715.0	-1058.5
7	SEG16	605.0	1058.5	47	COM1	-605.0	-1058.5
8	SEG15	495.0	1058.5	48	COM2	-495.0	-1058.5
9	SEG14	385.0	1058.5	49	COM3	-385.0	-1058.5
10	SEG13	275.0	1058.5	50	COM4	-275.0	-1058.5
11	SEG12	165.0	1058.5	51	COM5	-165.0	-1058.5
12	SEG11	55.0	1058.5	52	COM6	-55.0	-1058.5
13	SEG10	-55.0	1058.5	53	COM7	55.0	-1058.5
14	SEG9	-165.0	1058.5	54	COM8	165.0	-1058.5
15	SEG8	-275.0	1058.5	55	COM9	275.0	-1058.5
16	SEG7	-385.0	1058.5	56	COM10	385.0	-1058.5
17	SEG6	-495.0	1058.5	57	COM11	495.0	-1058.5
18	SEG5	-605.0	1058.5	58	COM12	605.0	-1058.5
19	SEG4	-715.0	1058.5	59	COM13	715.0	-1058.5
20	SEG3	-825.0	1058.5	60	COM14	825.0	-1058.5
21	SEG2	-940.0	1058.5	61	COM15	940.0	-1058.5
22	SEG1	-1055.0	1058.5	62	COM16	1055.0	-1058.5
23	VSS	-1175.0	1058.5	63	SEG40	1175.0	-1058.5
24	OSC1	-1295.0	1058.5	64	SEG39	1295.0	-1058.5
25	OSC2	-1268.0	853.7	65	SEG38	1259.8	-856.3
26	V1	-1259.8	733.7	66	SEG37	1259.8	-736.3
27	V2	-1259.8	613.7	67	SEG36	1259.8	-616.3
28	V3	-1259.8	498.7	68	SEG35	1259.8	-501.3
29	V4	-1259.8	383.7	69	SEG34	1259.8	-386.3
30	V5	-1259.8	273.7	70	SEG33	1259.8	-276.3
31	CL1	-1259.8	163.7	71	SEG32	1259.8	-166.3
32	CL2	-1259.8	53.7	72	SEG31	1259.8	-56.3
33	VDD	-1259.8	-56.3	73	SEG30	1259.8	53.7
34	M	-1259.8	-166.3	74	SEG29	1259.8	163.7
35	D	-1259.8	-276.3	75	SEG28	1259.8	273.7
36	RS	-1259.8	-386.3	76	SEG27	1259.8	383.7
37	R/W	-1259.8	-501.3	77	SEG26	1259.8	498.7
38	E	-1259.8	-616.3	78	SEG25	1259.8	613.7
39	DB0	-1259.8	-736.3	79	SEG24	1259.8	733.7
40	DB1	-1259.8	-856.3	80	SEG23	1259.8	853.7

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11.3. PIN Assignment

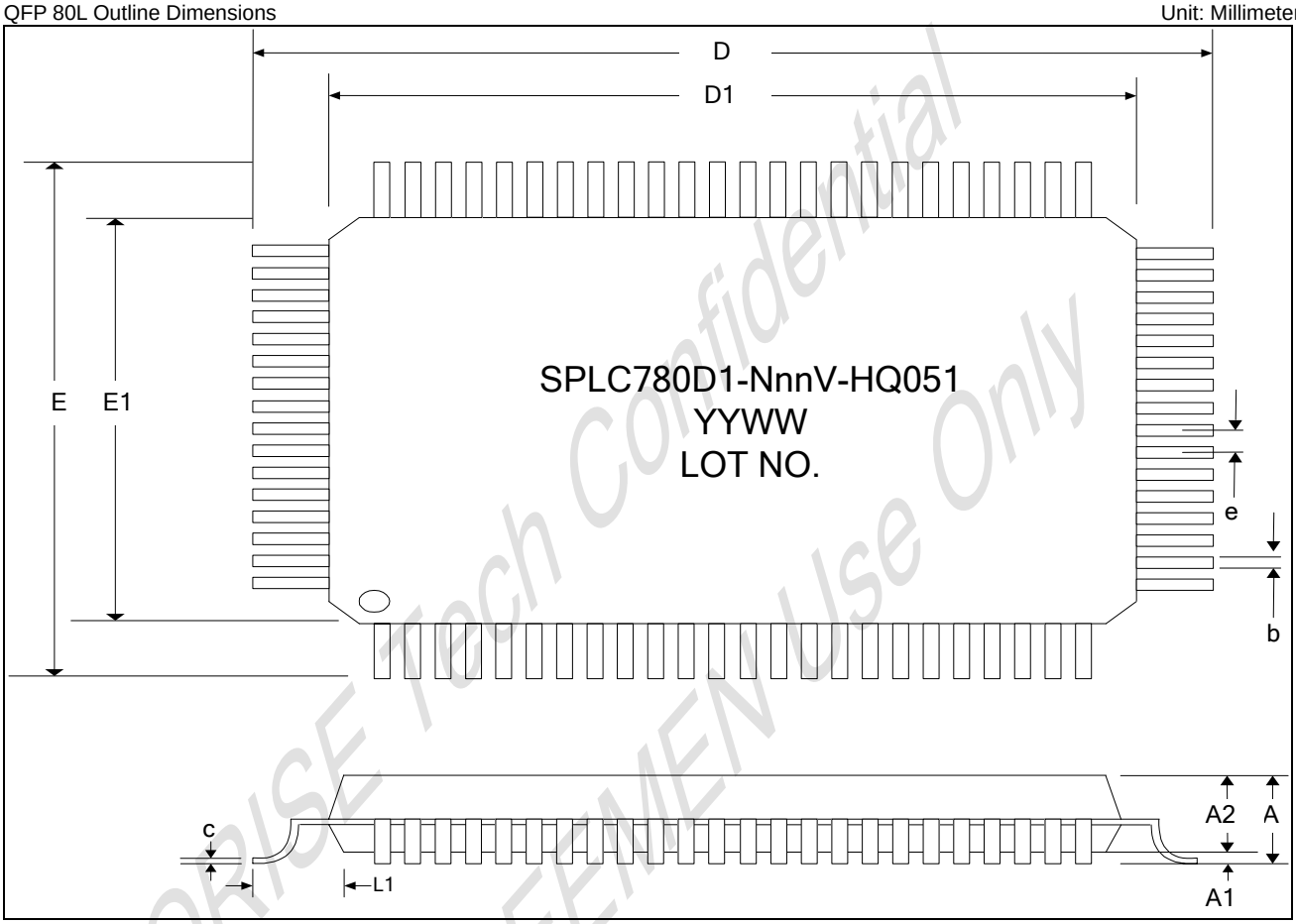
QFP 80L Top View



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11.4. Package Information (SPLC780D1-NnnV-HQ051)

QFP 80L Outline Dimensions Unit: Millimeter



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Symbol	Min.	Nom.	Max.	Unit
D		23.20 REF		Millimeter
D1		20.00 REF		Millimeter
E		17.20 REF		Millimeter
E1		14.00 REF		Millimeter
e		0.80 REF		Millimeter
b	0.30	0.35	0.45	Millimeter
A	-	-	3.40	Millimeter
A1	0.25	-	-	Millimeter
A2	2.50	2.72	2.90	Millimeter
c	0.11	0.15	0.23	Millimeter
L1		1.60 REF		Millimeter

12. LEAD FRAME PACKAGE PCB DESIGN AND MANUFACTURING GUIDELINES

12.1. Purpose

The purpose of this specification is to identify plastic surface mount devices (SMDs) those are sensitive to moisture-induced stress, so that they can be properly design PCB and assembly packaged, stored and handled to avoid subsequent mechanical damage during the assembly solder reflow attachment and /or repair operation.

12.2. Scope

12.2.1. PCB layout guideline

12.2.2. PCB process

12.2.3. Storage Condition and Period for Package

12.2.4. Recommended SMT Temperature Profile

12.3. Noun definition

12.3.1. NSMD: Non Solder Mask Defined

12.3.2. SMD: Solder Mask Defined

12.3.3. CSP: Chip scale Package

12.3.4. PCB :Printed Circuit Board

12.4. Responsibility unity:

ORISETECH Quality Assurance unity

12.5. Contents

12.5.1. Applicable documents

IPC-SM-782: Surface Mount Design & Land Pattern Standard

IPC-7351Generic Requirements for Surface Mount Design and Land Pattern Standard.

IPC-7525: Stencil Design Guidelines

J-STD-020: IPC/JEDEC Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Device

IPC JEDEC: J-STD-033A Standard for Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices

IPC-HDBK-001: Handbook & Guide to the Requirements of Soldered Electronic Assemblies with Amendment 1

IPC -6016: Qualification & Performance Specification for High Density Interconnect (HDI) Layers or Boards

IPC-STD-003: Solderability Tests for Printed Boards

JESD22-B111: Board Level Drop Test of Components for Handheld Electronic Products

JESD22-B110: Subassembly Mechanical Shock

IPC-A-610: Acceptability of Electronic Assemblies

12.5.2. PCB layout guideline

PCB designer comply with IPC-SM-782 and IPC-7095 requirements is recommended

12.5.3. PCB process

12.5.3.1. Board material

The Glass transition temperature (Tg) of Board material greater than 170 degree C is recommended for Pb-free and Green package.

12.5.3.2. Surface Finishes

In order to achieve high assembly yields, use of a surface finish that is planar

And has good solderability performance is important. Below methods are all known to provide an acceptable land pad surface.

*OSP (Organic Solderability Preservative)

*Nihau (Electroplated nickel /gold)

*Immersion Ag

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*Immersion Sn

12.5.3.3. Solder Paste: No clean flux is recommended.

12.5.3.4. Stencil Design Guidelines: Refer to IPC-7525 Stencil Design Guidelines process

12.5.3.5. Reflow Oven: Forced convection reflow with nitrogen is recommended for Pb-free and Green package..

12.5.3.6. Reflow profile: Using more than 8 zone oven is recommended for Pb-free and Green package.

12.5.3.7. To use IPC-A-610 is recommended for soldered electrical and electronic assemblies.

12.5.4. Storage condition and period for package

Orise technology evaluates all plastic surface mount devices (SMDs) to ICP/JEDEC J-STD-020A, moisture/reflow sensitivity classification for non-hermetic solid state surface mount devices, or refers to IPC JEDEC J-STD-033A Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices

12.5.4.1. The primary facts for the package storage include oxidation, static, and therefore, the following rules are recommended to be applied for the storage.

12.5.4.2. The storage temperature should be 25℃ ± 5℃, and the humidity should be in the range of 50% ± 10% R.H. after opening the dry pack.

After the dry bag is opened, devices that will be subjected to infrared reflow, vapor-phase reflow, or equivalent processing.

12.5.4.3. Must be:

a. Mounted within 168 hours(Level 3) and 72 hours(Level 4) at factory conditions of ≦ 30℃/ 60% R.H. or

b. Stored at ≦ 20% R.H.

12.5.4.4. Devices require baking, before mounting, if:

a. Humidity Indicator Card shown warning message when read at 25℃±5℃, or

b. 12.5.4.3 is not met.

12.5.4.5. If baking is required. Devices may be baking for:

a. 192 hour at 40℃+5℃/-0℃ and <5% R.H. for low temperature device containers, or

b. 24 hours at 125±5℃ for high temperature device containers

12.5.4.6. The storage condition should be consistent with the operation condition to prevent dewing phenomena.

12.5.4.7. The storage location should be kept away from water and smoke; an isolated area with positive pressure control is preferred.

12.5.4.8. For a long-term storage, it is recommended to keep in a container with Nitrogen in it.

12.5.4.9. Avoid heavy objects stacked on the pack.

12.5.4.10. Avoid the static damage; use an anti-static bag for the package.

12.5.5. The classification of moisture sensitivity for Orise's product packages are shown in the following

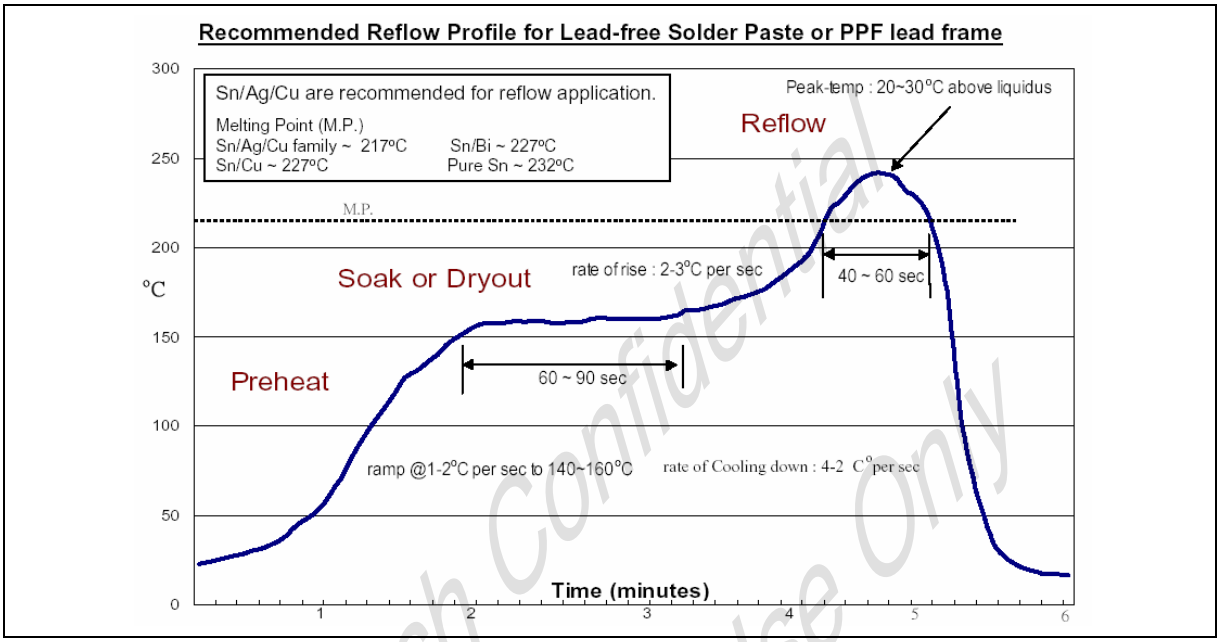
For Lead Free / Green Packages

Package	Moisture sensitivity level	Max. Reflow temperature	Floor life storage condition	Dry pack
QFP	LEVEL 3	255 +5/-0℃	168Hrs @ ≦ 30℃/ 60% R.H.	Yes

12.5.6. Recommended SMT Temperature Profile

This "Recommended" temperature profile is a rough guideline for SMT process reference. Most of ORISE leadframe base product choice Matte Tin and Sn/Bi for plating recipe. For PPF (Pre-Plated Frame) product with 63/37 solder paste, we recommend 240℃~245℃ for peak temperature.

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12.6. References

IPC:

http://www.ipc.org

*NEMI (National Electronics Manufacturing Initiative)

http://www.nemi.org

*HDPUG (High Density Package Users Group)

http://www.hdpug.org

*JEDEC (Joint Electronic Device Engineering Council)

http://www.jedec.org

*JEITA (Japan Electronic Industry Association)

http://www.jeita.org

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14. REVISION HISTORY

Date	Revision #	Description	Page
SEP. 21, 2007	0.1	Original	46

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